Mobility Anisotropy in Black Phosphorus MOSFETs With HfO_2 Gate Dielectrics

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***Abstract*— Precise measurements of the mobility anisotropy along high-symmetry crystal axes in black phosphorus (BP) MOSFETs are reported. Locally back-gated BP MOSFETs with 13-nm HfO_2 dielectric and channel length ranging from 0.3 to 0.7 μm are fabricated. A single BP flake of a uniform thickness is exfoliated and etched along armchair (AC) and zigzag (ZZ) crystal axes, and the orientations are confirmed using optical and transmission electron microscopy analyses. The hole and electron mobilities along each direction are extracted using the transfer length method. The AC-to-ZZ hole mobility ratio is found to increase from 1.4 (1.5) to 2.0 (2.9) as the sheet concentration increased from 5.1×10^{11} to 1.9×10^{12} cm^{-2} at room temperature (77 K). The room-temperature electron mobility anisotropy is found to be similar to that for holes with an AC-to-ZZ mobility ratio increasing from 1.4 to 2.1 from 5.1×10^{11} to 1.9×10^{12} cm^{-2} though electrons showed only a very weak temperature dependence. A Boltzmann transport model is used to explain the concentration- and temperature-dependent mobility anisotropies which can be well described using a charge center scattering model.**

***Index Terms*— Anisotropy, black phosphorus (BP), mobility, MOSFETs, phosphorene.**

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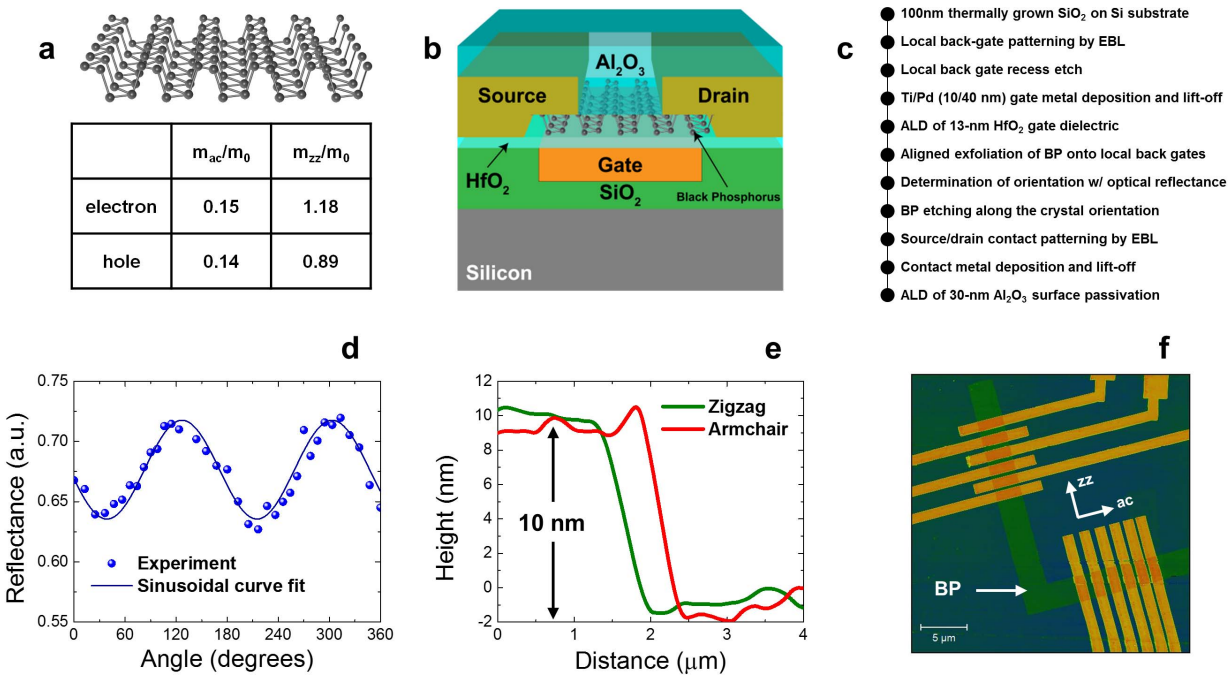
I. Introduction

2-D MATERIALS are a potential platform for numerous emerging device applications including scaled logic transistors, photonic devices, sensors, flexible electronics, and other innovative device concepts. Among the 2-D material options, black phosphorus (BP) [1] has recently emerged as a particularly promising layered semiconductor [2], [3] due to its unique material properties. BP has a tunable bandgap [4]–[6], high electron and hole mobility [2], [7]–[9], and in-plane effective mass anisotropy [7], [10], [11] due to its puckered crystal structure. These unique properties can be exploited in the design and optimization of electronic and optoelectronic devices. Since 2014, when a resurgent interest in BP devices occurred [2], [3], field-effect transistors (FETs) with drive current over 1 mA/ μm and transconductance over 300 μS/ μm have been demonstrated [12]–[14]. Furthermore, Te-doped BP has shown room-temperature hole mobility up to 1850 cm^2/Vs, which is the highest room-temperature mobility reported for any 2-D semiconductor [8]. The excellent mobility indicates that BP has the potential to outperform other 2-D semiconductors [15]–[17] and is particularly well suited for high-performance logic [18], [19], memory [20], and radio-frequency transistor applications [21]–[23]. Anisotropic effective mass is one of the key elements in BP [Fig. 1(a)], which leads to the variation of the mobility along different crystal orientations. According to [7], the effective mass of monolayer BP is over 6× larger along the zigzag (ZZ) crystal orientation compared to the armchair (AC) orientation for both electrons and holes. This large ratio can cause a great variation in the properties of randomly oriented BP FETs [3], [12], [24], and therefore controlling the transport orientation is essential for any practical application. Orientation control has recently been used to demonstrate BP FETs with enhanced performance [25]; however, to date, no comprehensive experimental studies of thin-film BP carrier mobility have been reported. In [3], the angle-dependent transport in BP was analyzed; however, the electric field was not well isolated along the transport direction, likely leading to an underestimation of the mobility anisotropy. Other reports of the mobility where the crystal orientation in a BP FET was well controlled either utilized a thick bulk crystal [26] or investigated one carrier type in thin-film BP at a single carrier concentration [10], [27]. None of the previous works have investigated the field-effect mobility crystal anisotropy in thin-film BP as a function of



	m_{ac}/m_0	m_{zz}/m_0
electron	0.15	1.18
hole	0.14	0.89

Fig. 1. (a) Diagram of a single monolayer of BP and a list of the asymmetric crystal parameters for few-layer BP [7]. (b) Cross-sectional view of a typical locally back-gated BP MOSFET. (c) BP MOSFET fabrication process sequence. (d) Angular dependence of optical reflectance for BP devices used in this paper. (e) AFM line scan of BP channel along the AC and ZZ directions. (f) False-color AFM image of BP right-angle device structures along the ZZ and AC crystal directions.

carrier type, sheet concentration, and temperature. Finally, no prior studies on BP mobility anisotropy have been performed in realistic FET geometries using high-κ dielectrics.

In this paper, we present a comprehensive study of BP electron and hole mobility in a scaled FET geometry with local backgates and HfO_2 gate dielectrics. This work is performed on a single BP flake that is etched along AC and ZZ orientations and shows how the crystal orientation significantly influences the electrical transport. Scanning transmission electron microscopy (STEM) was performed on the same device to confirm the crystal directions. We investigate the effect of carrier concentration and temperature on the BP electron and hole mobility along high-symmetry crystal axes. We also confirm the experimental trends by using a Boltzmann transport model to study the effect of scattering on BP electron and hole mobility anisotropy between different directions.

II. Experiment

A cross-sectional diagram of a typical BP FET with locally back-gated structure is shown in Fig. 1(b). The process flow used for device fabrication is illustrated in Fig. 1(c). Device fabrication started with 100 nm of thermally grown SiO_2 on a Si wafer. Local backgates were patterned by using electron-beam lithography (EBL) after alignment mark formation. Then, the SiO_2 was etched using a combination of dry and wet etching and Ti (10 nm)/Pd (40 nm) was deposited to form a buried gate electrode. After lifting off the gate metal, 13 nm of HfO_2 was deposited using atomic layer deposition (ALD) at 300 °C to form the gate dielectric, and BP was exfoliated, aligned, and transferred onto the local backgates. Next, as shown in Fig. 1(d), optical reflectance was used to determine the crystal orientation of the flakes before patterning the source and drain contacts. Due to the anisotropic nature of BP, the optical reflectance varies with the crystallographic orientation. A linearly polarized white light was used to illuminate BP flakes and then the reflectance was measured at different polarization angles (changing from 0° to 360°). The minimum reflectance corresponds to the maximum conductivity, hence lower effective mass. After determining the high-symmetry crystal axes, a right-angle structure was etched along the ZZ and AC crystal directions using an Ar plasma (100 W at 150 mTorr) for 80 s. Next, source and drain contacts were patterned by EBL in the transfer length method (TLM) geometry with the separations ranging from 0.3 to 0.7 μm. Then, Ti (10 nm)/Au (90 nm) contacts were deposited and lifted off to form the Ohmic contacts. Ti, which has a midgap work function, was used as the contact metal to allow both electron and hole conductivity to be explored in the same device. Finally, 30 nm of Al_2O_3 was deposited by ALD at 200 °C on the entire structure to passivate the devices, where Al_2O_3 was used to ensure ambipolar behavior, as has been demonstrated in [13], [28]. After completing the device fabrication, atomic force microscopy (AFM) was used to determine the thickness of BP which was roughly 10 nm thick in both the AC and ZZ regions of the device, as shown in Fig. 1(e). A false-color AFM image of the completed device structure is shown in Fig. 1(f).

After fabrication and characterization of the FETs, the crystal orientation was further confirmed using STEM. In order to measure the BP channel orientations, film thicknesses, and chemical compositions of both the AC- and ZZ-oriented FETs, two TEM cross-sectional lamellas were prepared from the right-angle TLM structure shown in Fig. 1(f) using a focused ion beam and subsequently inserted into a STEM. It is

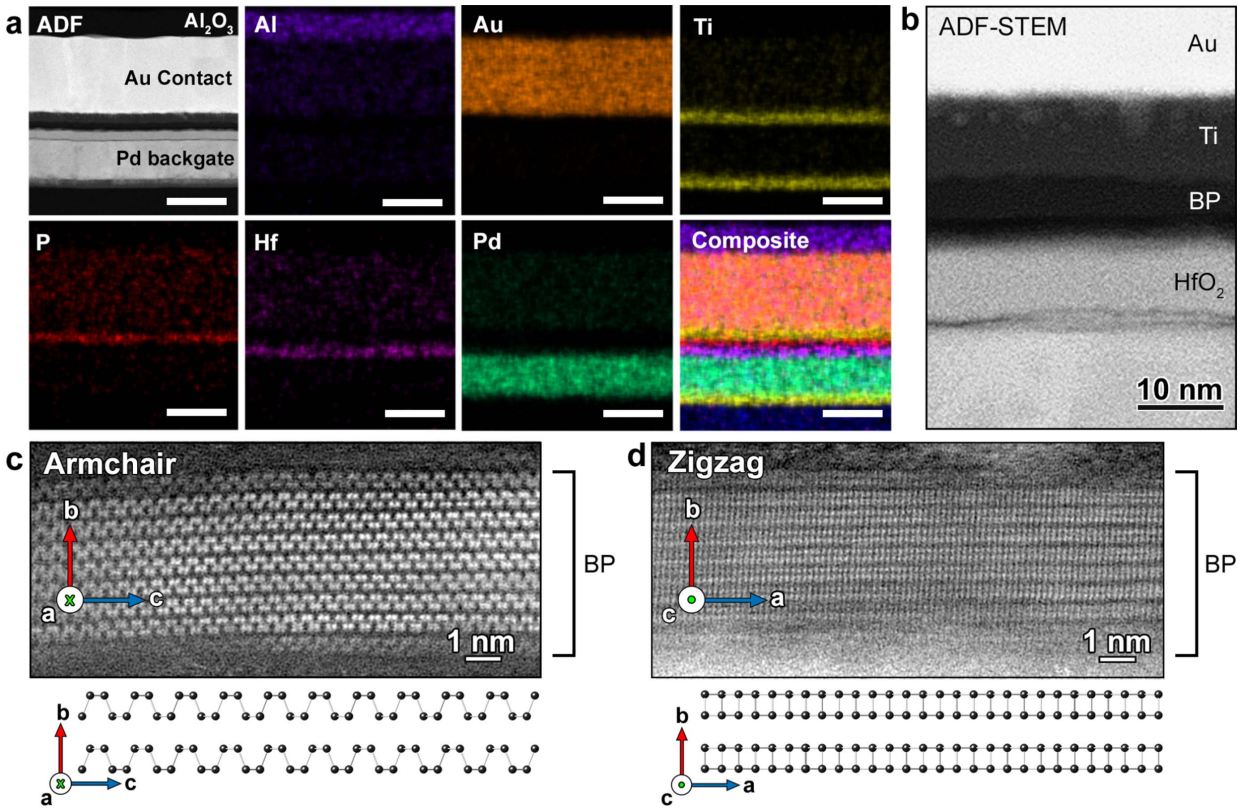


Fig. 2. (a) Low-magnification STEM-EDX elemental maps showing components of the BP MOSFET along with the corresponding ADF-STEM image of the scanned area. Scale bars are 40 nm. (b) Intermediate magnification ADF-STEM image of the BP channel and its surrounding layers. (c) Atomic resolution ADF-STEM image of the BP channel for the MOSFET with channel oriented along the [100] AC direction. (d) Atomic resolution ADF-STEM image of the BP channel for the MOSFET with channel oriented along the [010], ZZ direction. Ball-and-stick models of BP in the two orientations are shown below the images for comparison. Images in (c) and (d) have been low-pass filtered to limit information below 0.9 Å.

important to note that because the TEM lamella preparation is necessarily destructive, all electrical characterization on the TLM devices was performed prior to the STEM analysis. For this analysis, an aberration-corrected FEI Titan G2 60-300 STEM equipped with a Super-X energy dispersive X-ray (EDX) spectrometer and operating at 200 keV was used. The electron probe was corrected prior to image collection to achieve 0.9-Å spatial resolution. Fig. 2(a) shows low-magnification STEM-EDX elemental maps of the AC-oriented FET in which each layer of the cross-sectionally cut device can be chemically identified and compared with the device schematic is shown in Fig. 1(b). Fig. 2(b) shows an annular dark-field (ADF)-STEM image of the BP channel and its surrounding layers. Here, Z-contrast, which primarily differentiates the intensity in the ADF-STEM image between different layers of the FET, enables measurement of the thicknesses of the HfO_2 dielectric layer, BP (pristine and oxidized) channel, and surface roughness of the HfO_2. Although not shown, the ZZ-oriented FET that was fabricated using the same BP flake and device fabrication procedure as the AC-oriented device possesses the same chemical information and layer thicknesses as observed in Fig. 2(a) and (b). Fig. 2(c) and (d) shows atomic resolution images of the BP channel along the [100] (AC) and [010] (ZZ) directions, respectively, as acquired from the two, respectively, oriented TEM lamellas [29]. Based on the sample tilt in the STEM required to reach the AC and ZZ zone axes for the two, respectively, oriented samples, the crystallographic orientation of the channels in each FET was confirmed to be within 15° of the expectations based on optical reflectance measurements. In addition, the number of pristine layers (9 ± 1 layers), as determined by counting the crystalline layers, was determined by visual inspection of both images.

III. Results and Discussion

All electrical measurements were performed under vacuum (base vacuum $\sim 10^{-5}$ Torr) in a Lakeshore CPX-VF cryogenic probe station using an Agilent B1500A semiconductor parameter analyzer. Typical output and transfer characteristics of BP FETs with source-drain contact spacing L_{ch} of 0.4 μm are shown in Fig. 3, and these results demonstrate the ambipolar behavior of the BP FETs with Ti contacts, showing that both electron and hole conductivity can be achieved within a single device. The results from devices with other contact separations using the TLM geometry in Fig. 1 showed similar characteristics. Fig. 3(a) and (b) shows a comparison between BP FETs with AC orientation and ZZ orientation where the bias voltages have been chosen to obtain n-type conductivity. The AC-orientated devices clearly show a higher current drive than the ZZ-orientated devices. The transfer characteristics in

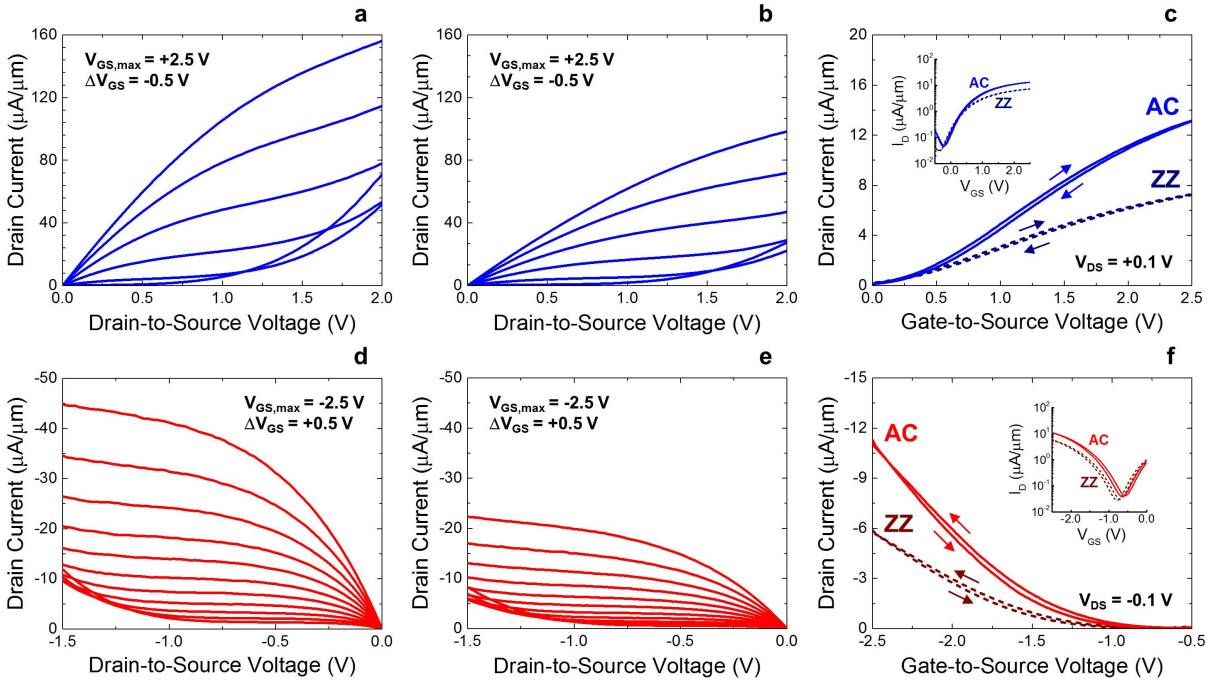


Fig. 3. Output characteristics for BP (a) and (b) n-MOSFETs and (d) and (e) p-MOSFETs with Ti/Au contacts and S/D separation of 0.4 μm with transport direction along the (a) and (d) AC and (b) and (e) ZZ crystal directions. (c) and (f) Transfer characteristics for the same BP MOSFETs as in (a) and (b) and (d) and (e), respectively. For each crystal direction, the n-MOSFET and p-MOSFET characteristics were measured on the same device; only the bias configuration was changed. For (c) and (f), both up and down sweeps are shown, indicating minimal hysteresis in the transfer characteristics. Insets: transfer characteristics on a semilog scale.

Fig. 3(c) along the high-symmetry crystal axes also confirm a similar trend. Fig. 3(d)–(f) shows results from the same device, where the bias voltages have been chosen to achieve p-type conductivity. Similar to the n-channel case, the p-channel devices show higher current drive along the AC direction. Both n- and p-FET devices show only a very small hysteresis in the transfer characteristics, suggesting that accurate mobility extraction can be achieved in these devices.

In short-channel FETs, in order to extract the field-effect mobility, the contact resistance must be carefully determined and subtracted using the TLM. The total width-scaled device resistance R_{total} can be determined using

$$R_{\text{total}} W = \frac{L_{ch}}{\mu C_{ox} |V_{\text{GS}} - V_{\text{th}}|} + R_C W \tag{1}$$

where μ is the mobility, C_{ox} is the gate capacitance per unit area, V_{th} is the threshold voltage, R_C is the contact resistance, and W is the channel width.

The value of V_{th} was determined from the I_D versus V_{GS} curves, at $|V_{\text{DS}}| = 10$ mV, using the constant current method. In this method, the threshold voltage was determined as the gate voltage at which $I_D \times L_{ch}/W = 20$ nA/μm, where I_D is the drain current per unit width. The value of 20 nA/μm was chosen since it corresponded closely to the point at which the second derivative of I_D versus V_{GS}, $d^2 I_D / dV_{\text{GS}}^2$, was a maximum [30]. The threshold was determined using this method for both pFETs and nFETs of both orientations, and for all source-to-drain spacings. Since the total fabrication process involved short (a few hours) but nonnegligible exposure to ambient atmosphere, a thin layer (3–5 nm) of phosphorus oxide forms between BP and HfO_2 [5], [31], which needs to be considered in determining C_{ox}. Atomic resolution STEM-EELS data also indicate the distortions on the bottom of Fig. 2(c) are phosphorus oxide. The thickness of the phosphorus oxide layer in this device is ~5 nm which is shown in the cross-sectional STEM in Fig. 2(b), while the HfO_2 has a thickness of 13 nm. Based upon the STEM analysis, the average surface roughness between the HfO_2 and phosphorus oxide layer was determined to be ~3 nm. This surface roughness creates gaps between the HfO_2 and phosphorus oxide leading to an overall reduction in the gate-stack capacitance. In our capacitance extraction procedure, we utilized the previously determined [32] dielectric constant of 16.6 for our ALD HfO_2, and we further assumed an out-of-plane dielectric constant of 4 for phosphorus oxide. Using these parameters, a value of $C_{ox} = 0.373$ μF/cm^2 was extracted. We did not take into account quantum capacitance when calculating the total capacitance, which is a reasonable assumption in the strong inversion limit. We note that the atmospheric exposure during processing was shorter than described in [33] and [34], where significant transport degradation was observed, and the results in Fig. 2 show that the macroscopic crystal properties of the BP are preserved. Furthermore, while the presence of the phosphorus oxide layer could still affect the mobility and anisotropy values extracted, such an interfacial oxide layer is also typical in silicon-based MOSFETs with high-κ dielectrics [35].

The linear-regime output characteristics of BP n-FETs along the AC and ZZ crystal orientation for channel length ranging from 0.3 to 0.7 μm are shown in Fig. 4(a). These characteristics confirm the linearity of the contacts at low drain-to-source bias and also show the expected trend of increasing current for

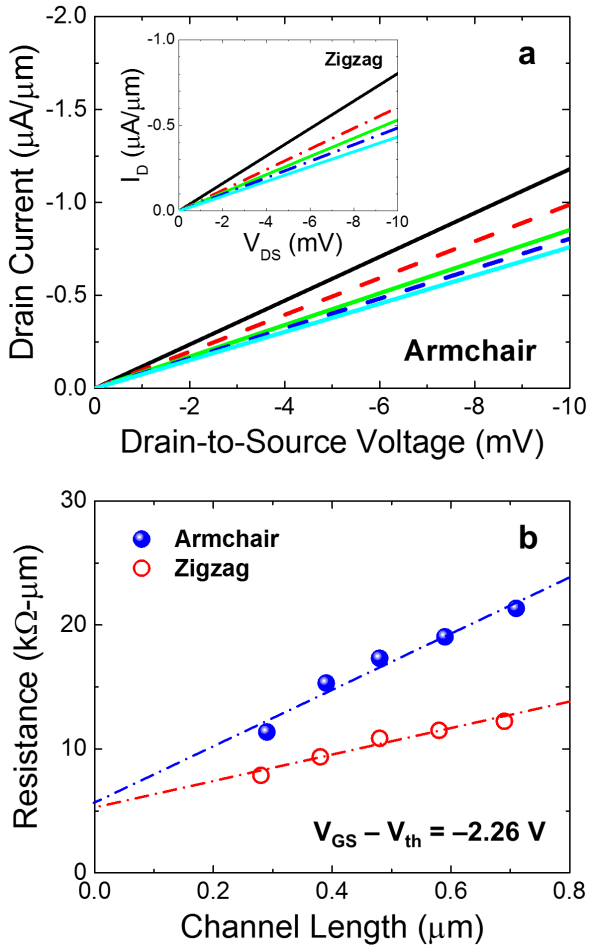


Fig. 4. (a) Drain current I_D versus drain-to-source voltage V_{DS} for contacts separations of 0.7 μm (cyan solid line), 0.6 μm (blue dashed line), 0.5 μm (green solid line), 0.4 μm (red dashed line), and 0.3 μm (black solid line) for a BP p-MOSFET along the AC direction. Inset: same plot for a BP p-MOSFET along the ZZ direction. $V_{GS} - V_{th} = -2.26$ V. (b) Total resistance R_{tot} versus channel length L_{ch} at $V_{GS} - V_{th} = -2.26$ V and $V_{DS} = -10$ mV along AC (blue closed circles) and ZZ (red open circles) for the same device as in (a). Field-effect mobility along each crystal orientation can be extracted from the slope of the linear fit.

shorter channel lengths. A good contact linearity was observed for all bias conditions and temperatures reported in this paper. To extract the mobility, total resistance was extracted for both crystal orientations as a function of channel length at $|V_{DS}| = 10$ mV, and these results are plotted in Fig. 4(b). The different slopes verify the different sheet resistance along the two orientations and assuming that the carrier concentration is constant for each channel length, the mobility can be extracted from the slope. As expected, the mobility along the AC orientation is higher than the ZZ orientation. Interestingly, Fig. 4(b) also shows that there is not a substantial difference between the contact resistance along different orientations, which is likely due to the fact that the specific contact resistivity of the Schottky contact is determined by the out-of-plane effective mass, which is the same in both cases [36], [37]. In [37], it is shown that the channel portion underneath the contact in Schottky-contacted 2-D materials plays a significant role in determining the contact resistance.

The mobility μ of electrons and holes in the BP devices used in this paper was extracted using

$$\mu = \frac{1}{R_{sh} C_{ox} |V_{GS} - V_{th}|} \tag{2}$$

where R_{sh} is the sheet resistance which is extracted from the slope of curves similar to Fig. 4(b), and $|V_{GS} - V_{th}|$ is the gate overdrive voltage. The carrier concentration, n or p, is calculated as $C_{ox}|V_{GS} - V_{th}|/q$, where q is the electronic charge, where this relation applies to either electrons or holes. This estimate for the carrier concentration is valid in the strong inversion limit, which occurs when $|V_{GS} - V_{th}| \gg kT/q$. For our devices, at the lowest carrier concentration of 5.1×10^{11} cm^{-2}, $|V_{GS} - V_{th}| > 0.2$ V, and therefore, this condition is satisfied for all concentrations evaluated in this paper. Both low and high carrier density regimes were observed for electron mobility; however, due to the high threshold voltage, only the low carrier density regime was observed in the case of hole transport. The hole effective mass in BP along each crystallographic orientation is lower than the electron effective mass [Fig. 1(a)]; therefore, it is expected that the hole mobility should be higher than the electron mobility, and this expectation is confirmed with the experimental data shown in Fig. 5(a) and (b). For instance, at a fixed overdrive voltage, $|V_{GS} - V_{th} = 1|$ V, the hole mobility along AC direction (ZZ) is 1.8× (1.9×) higher than the electron mobility along the same crystal orientation. The AC mobility for both electrons and holes is also higher than the ZZ mobility by ∼2× over a wide range of carrier concentrations. We note that the somewhat lower overall mobility in this paper comparing to [3] and [8] could have several sources. First of all, our samples were prepared in an ambient atmosphere which leads to oxidation of the BP at the BP/dielectric interface which can lead to interface trap formation. Second, our devices utilize HfO_2, a high-κ dielectric, which can degrade the carrier mobility due to the soft-optical phonon scattering [38]. Finally, both the local backgate and the BP oxidation can lead to surface roughness at the BP/dielectric interface, which is apparent in the cross-sectional STEM image in Fig. 2(b).

In order to explore the mobility characteristics further, the concentration-dependent mobility was extracted as a function of temperature ranging from 77 to 295 K. As shown in Figs. 6 and 7, both the AC and ZZ mobilities show weak temperature-dependent behavior with the mobilities increasing somewhat as the temperature is reduced. At a fixed hole sheet concentration of 1.9×10^{12} cm^{-2}, the AC (ZZ) hole mobility changed from 165 (83) cm^2/Vs at 295 K to 310 (106) cm^2/Vs at 77 K while the AC (ZZ) electron mobility at the same corresponding electron sheet concentration changes from 104 (49) cm^2/Vs at 295 K to 145 (66) cm^2/Vs at 77 K. The mobility shows a power-law dependence of $\mu \propto T^{-x}$, where $x = 0.51 \pm 0.06$ (0.22 ± 0.04) for the AC (ZZ) hole mobility, and $x = 0.20 \pm 0.05$ (0.21 ± 0.01) for the AC (ZZ) electron mobility. The mobility variation as a function of temperature is stronger along the AC direction compared to the ZZ direction for holes but not for electrons. Both the values and the temperature dependences of the mobilities suggest that they are limited by extrinsic scattering mechanisms.

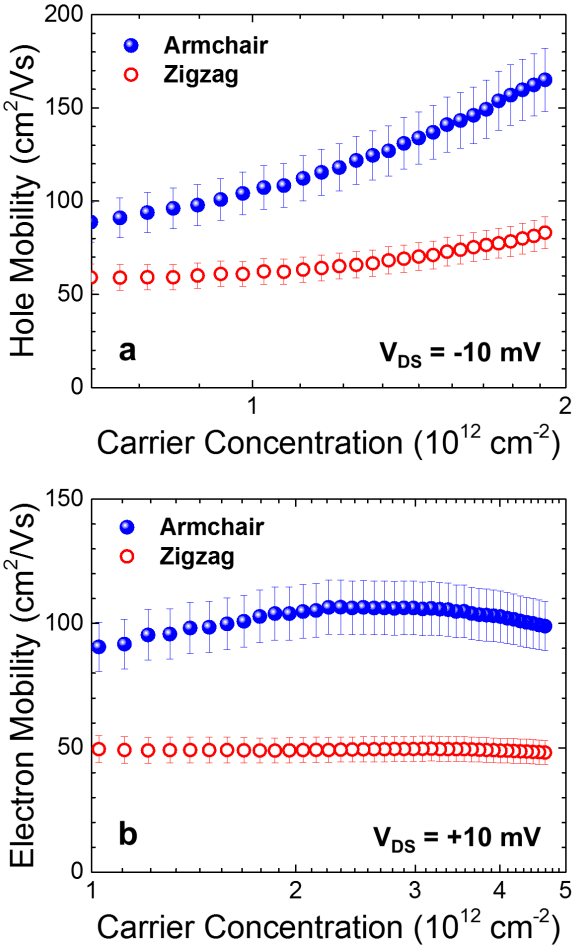


Fig. 5. (a) Room-temperature hole mobility versus hole concentration for a BP p-MOSFET along the AC (blue closed circles) and ZZ (red open circles) crystal orientations. (b) Room-temperature mobility electron mobility versus electron concentration for a BP n-MOSFET along the AC (blue closed circles) and ZZ (red open circles) crystal orientations. For each crystal direction, the hole and electron mobilities were measured on the same device; only the bias configuration was changed.

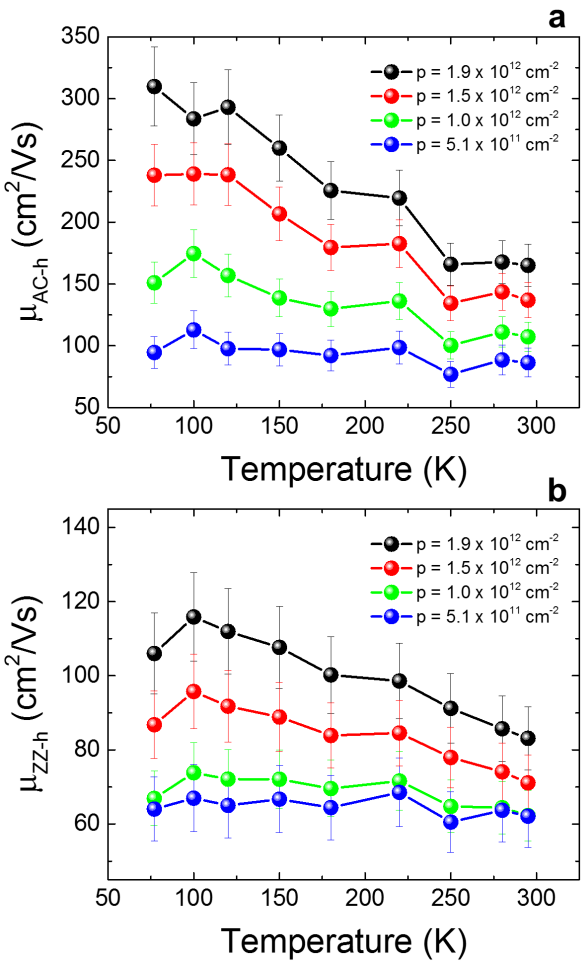


Fig. 6. Hole mobility versus temperature in (a) AC and (b) ZZ directions. Black, red, green, and blue colors correspond to hole sheet concentration of 1.9×10^{12} cm^{-2}, 1.5×10^{12} cm^{-2}, 1×10^{12} cm^{-2}, and 5.1×10^{11} cm^{-2}, respectively.

While these mobilities are much lower than those achieved on h-BN-passivated samples [39], they are typical values of various reports using high-κ gate dielectrics [40], which are clearly more relevant for future commercial applications.

To analyze the measured anisotropic carrier mobilities further we apply a recently developed model that is based on the Boltzmann transport equation and takes the anisotropy of the parabolic conduction and valence band extrema fully into account. The basic model and its application to BP mobilities were described in [11] and [41]; however, those studies only described the mobility anisotropy at high carrier concentration and lower temperatures. In the following, we discuss the salient features of this model that are relevant to the experimental data reported in this paper.

First, a scattering of a mobile charge carrier due to its interaction with a fixed charge center (an impurity or other defect) strongly favors small-angle scattering. Consequently, only a fraction of the final-state phase space (a constant energy ellipse) is relevant for this scattering process. This implies that scattering due to charge centers is less sensitive to the anisotropy of the material that would be, for example, an angle-independent (velocity randomizing) scattering mechanism. Second, the degree to which small-angle scattering is favored depends on the screening of the Coulomb interaction by the mobile charge carriers. Changes in the carrier concentration, therefore, affect the mobility anisotropy. For the carrier concentrations and the relatively high temperature relevant for this paper, the screening parameter is approximately proportional to the carrier concentration, and so screening increasingly reduces the bias toward small-angle scattering when the carrier concentration increases. This results in increasing mobility anisotropy with increasing carrier density.

Evidently, mobilities limited by charge center scattering depend linearly on the density of charged impurities or other defects. While it appears to be the case that the carrier mobilities in the samples explored in this paper are limited by an extrinsic scattering mechanism, and charge center scattering is a strong candidate, there is no reason to believe that the charge state of the impurities or defects remains constant as

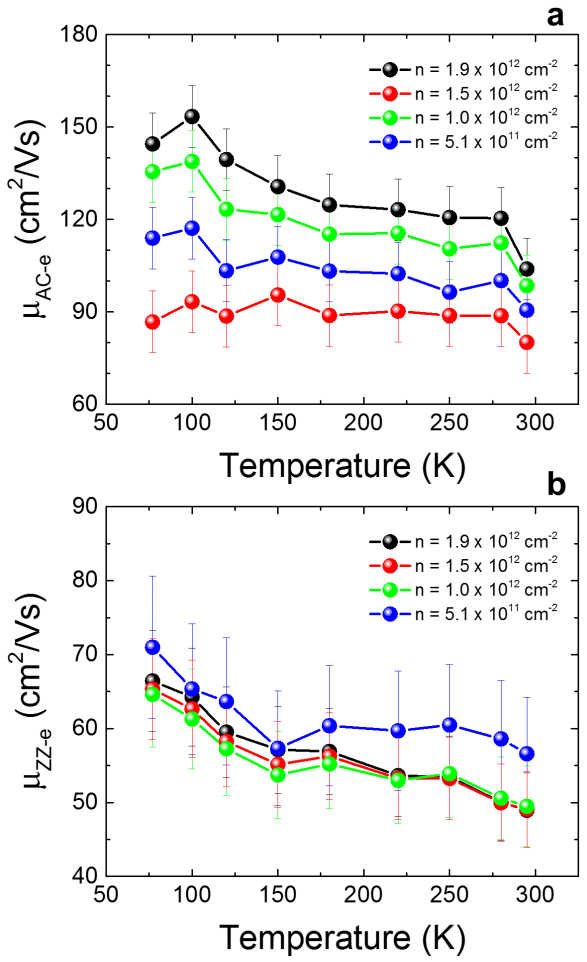


Fig. 7. Electron mobility versus temperature in (a) AC and (b) ZZ directions. Black, red, green, and blue colors correspond to electron sheet concentration of 1.9 × 10^{12} cm^{-2}, 1.5 × 10^{12} cm^{-2}, 1 × 10^{12} cm^{-2}, and 5.1 × 10^{11} cm^{-2}, respectively.

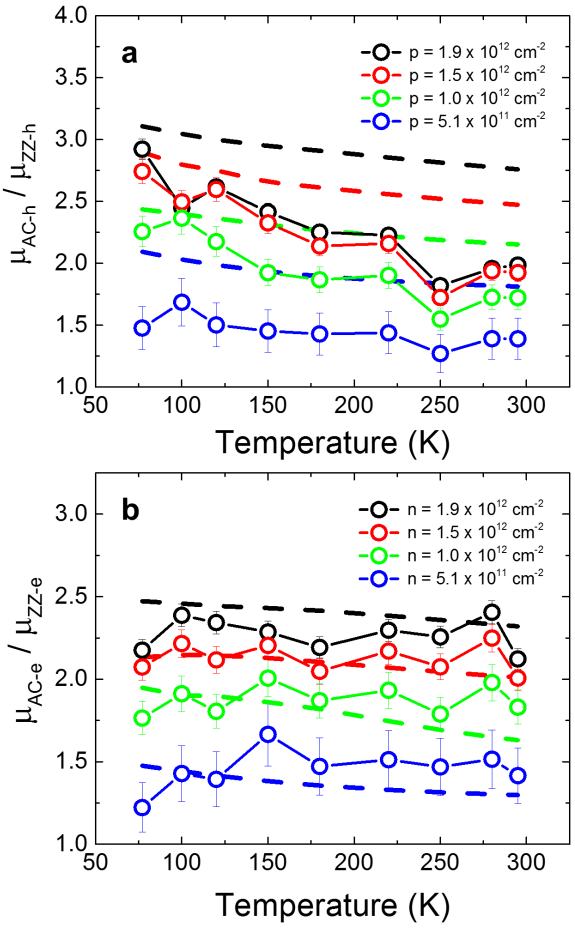


Fig. 8. AC-to-ZZ mobility ratio, μ_{AC}/μ_{ZZ}, for (a) holes and (b) electrons as a function of temperature T ranging from 77 to 295 K. Black, red, green, and blue colors correspond to hole sheet concentration p and electron sheet concentration n of 1.9 × 10^{12}, 1.5 × 10^{12}, 1 × 10^{12}, and 5.1 × 10^{11} cm^{-2}, respectively. Open symbols: experimental results. Dashed lines: calculated results.

the carrier concentration is varied and the quasi-Fermi level is swept through the band structure. Consequently, we focus our comparison of the calculations to the experimental results on the mobility anisotropy ratio rather than on the individual mobilities. The anisotropy ratio, of course, is independent of the density of charge centers.

The calculated results are shown together with the experimentally determined mobility ratios in Fig. 8. A reasonable agreement is found, considering the uncertainty of the effective mass parameters, which may deviate from the monolayer values due to the fact that the structures characterized experimentally contained multilayer BP, and the effective masses are expected to vary with the number of monolayers. Furthermore, charge center scattering is sensitive to the location of the charge centers, as was explored in [11] and [41]. Here, we restricted the calculations to charge centers located within the BP layer. Finally, it is possible that other scattering mechanisms contribute to the measured mobility values. Surface roughness scattering may be an additional extrinsic mechanism that impacts the carrier mobilities, particularly at high carrier concentration when the vertical electric field is the largest.

IV. Conclusion

In conclusion, we have reported a comprehensive study of the mobility anisotropy in BP MOSFETs with HfO_2 gate dielectrics. Using a right-angled test structure patterned on a single flake, the mobility has been analyzed as a function of high-symmetry crystal direction, temperature, carrier type, and concentration. The extracted room-temperature field-effect mobility was found to be higher in the AC versus ZZ direction, and the anisotropy ratio was found to increase with increasing sheet carrier concentration for both electrons and holes in the low-concentration regime. We also found that the hole mobility anisotropy increases with decreasing temperature, while the electron mobility anisotropy was relatively flat versus temperature. In all cases, the hole mobility was found to be higher than the electron mobility, consistent with the reported BP electron and hole effective mass. The temperature- and concentration-dependent mobility anisotropy can be understood using a theoretical Boltzmann transport model. This paper has important implications for future electronic and photonic devices based upon BP.

REFERENCES

[1] P. W. Bridgman, "Two new modifications of phosphorus," *J. Amer. Chem. Soc.*, vol. 36, no. 7, pp. 1344–1363, 1914.

[2] L. Li *et al.*, "Black phosphorus field-effect transistors," *Nature Nanotechnol.*, vol. 9, no. 5, pp. 372–377, Mar. 2014.

[3] H. Liu *et al.*, "Phosphorene: An unexplored 2D semiconductor with a high hole mobility," *ACS Nano*, vol. 8, no. 4, pp. 4033–4041, Mar. 2014.

[4] V. Tran, R. Soklaski, Y. Liang, and L. Yang, "Layer-controlled band gap and anisotropic excitons in few-layer black phosphorus," *Phys. Rev. B, Condens. Matter*, vol. 89, no. 23, p. 235319, 2014.

[5] B. Deng *et al.*, "Efficient electrical control of thin-film black phosphorus bandgap," *Nature Commun.*, vol. 8, Apr. 2017, Art. no. 14474.

[6] S. Das, W. Zhang, M. Demarteau, A. Hoffmann, M. Dubey, and A. Roelofs, "Tunable transport gap in phosphorene," *Nano Lett.*, vol. 14, no. 10, pp. 5733–5739, Aug. 2014.

[7] J. Qiao, X. Kong, Z.-X. Hu, F. Yang, and W. Ji, "High-mobility transport anisotropy and linear dichroism in few-layer black phosphorus," *Nature Commun.*, vol. 5, Jul. 2014, Art. no. 4475.

[8] B. Yang *et al.*, "Te-doped black phosphorus field-effect transistors," *Adv. Mater.*, vol. 28, no. 2, pp. 9408–9415, Aug. 2016.

[9] S. Das, M. Demarteau, and A. Roelofs, "Ambipolar phosphorene field effect transistor," *ACS Nano*, vol. 8, no. 11, pp. 11730–11738, Oct. 2014.

[10] F. Xia, H. Wang, and Y. Jia, "Rediscovering black phosphorus as an anisotropic layered material for optoelectronics and electronics," *Nature Commun.*, vol. 5, Jul. 2014, Art. no. 4458.

[11] Y. Liu, T. Low, and P. P. Ruden, "Mobility anisotropy in monolayer black phosphorus due to scattering by charged impurities," *Phys. Rev. B, Condens. Matter*, vol. 93, no. 16, p. 165402, 2016.

[12] L. Li, M. Engel, D. B. Farmer, S.-J. Han, and H.-S. P. Wong, "High-performance p-type black phosphorus transistor with scandium contact," *ACS Nano*, vol. 10, no. 4, pp. 4672–4677, Mar. 2016.

[13] N. Haratipour and S. J. Koester, "Ambipolar black phosphorus MOSFETs with record n-channel transconductance," *IEEE Electron Device Lett.*, vol. 37, no. 1, pp. 103–106, Jan. 2016.

[14] L. M. Yang *et al.*, "Few-layer black phosporous PMOSFETs with BN/AI_2O_3 bilayer gate dielectric: Achieving $I_{on} = 850\mu A/\mu m$, $g_m = 340\ \mu S/\mu m$, and $R_c = 0.58\ k\Omega{\cdot}\mu m$," in *IEDM Tech. Dig.*, Dec. 2016, pp. 5.5.1–5.5.4.

[15] L. Yang, R. T. P. Lee, S. S. P. Rao, W. Tsai, and P. D. Ye, "10 nm nominal channel length MoS_2FETs with EOT 2.5 nm and 0.52 $mA/\mu m$ drain current," in *Proc. 73rd Annu. Device Res. Conf. (DRC)*, Jun. 2015, pp. 237–238.

[16] X. Zou *et al.*, "Interface engineering for high-performance top-gated MoS_2 field-effect transistors," *Adv. Mater.*, vol. 26, no. 36, pp. 6255–6261, 2014.

[17] C. D. English, K. K. H. Smithe, R. L. Xu, and E. Pop, "Approaching ballistic transport in monolayer MoS_2 transistors with self-aligned 10 nm top gates," in *IEDM Tech. Dig.*, Dec. 2016, pp. 5.6.1–5.6.4.

[18] Y. Su, C. U. Kshirsagar, M. C. Robbins, N. Haratipour, and S. J. Koester, "Symmetric complementary logic inverter using integrated black phosphorus and MoS_2 transistors," *2D Mater.*, vol. 3, no. 1, 2016, Art. no. 011006.

[19] S. P. Koenig *et al.*, "Electron doping of ultrathin black phosphorus with Cu Adatoms," *Nano Lett.*, vol. 16, no. 4, pp. 2145–2151, Mar. 2016.

[20] H. Tian *et al.*, "A dynamically reconfigurable ambipolar black phosphorus memory device," *ACS Nano*, vol. 10, no. 11, pp. 10428–10435, 2016.

[21] H. Wang *et al.*, "Black phosphorus radio-frequency transistors," *Nano Lett.*, vol. 14, no. 11, pp. 6424–6429, Oct. 2014.

[22] W. Zhu *et al.*, "Flexible black phosphorus ambipolar transistors, circuits and AM demodulator," *Nano Lett.*, vol. 15, no. 3, pp. 1883–1890, Feb. 2015.

[23] W. Zhu, S. Park, M. N. Yogeesh, K. M. McNicholas, S. R. Bank, and D. Akinwande, "Black phosphorus flexible thin film transistors at gighertz frequencies," *Nano Lett.*, vol. 16, pp. 2301–2306, Mar. 2016.

[24] N. Haratipour, S. Namgung, S.-H. Oh, and S. J. Koester, "Fundamental limits on the subthreshold slope in Schottky source/drain black phosphorus field-effect transistors," *ACS Nano*, vol. 10, no. 3, pp. 3791–3800, 2016.

[25] N. Haratipour, S. Namgung, R. Grassi, T. Low, S.-H. Oh, and S. J. Koester, "High-performance black phosphorus MOSFETs using crystal orientation control and contact engineering," *IEEE Electron Device Lett.*, vol. 38, no. 5, pp. 685–688, May 2017.

[26] Y. Akahama, S. Endo, and S. Narita, "Electrical properties of black phosphorus single crystals," *J. Phys. Soc. Jpn.*, vol. 52, no. 6, pp. 2148–2155, 1983.

[27] J. Tao *et al.*, "Mechanical and electrical anisotropy of few-layer black phosphorus," *ACS Nano*, vol. 9, no. 11, pp. 11362–11370, 2015.

[28] H. Liu, A. T. Neal, M. Si, Y. Du, and P. D. Ye, "The effect of dielectric capping on few-layer phosphorene transistors: Tuning the Schottky barrier heights," *IEEE Electron Device Lett.*, vol. 35, no. 7, pp. 795–797, Jul. 2014.

[29] R. J. Wu *et al.*, "Atomic and electronic structure of exfoliated black phosphorus," *J. Vac. Sci. Technol. A, Vac. Surf. Films*, vol. 33, no. 6, 2015, Art. no. 060604.

[30] A. Ortiz-Conde, F. J. G. Sánchez, J. J. Liou, A. Cerdeira, M. Estrada, and Y. Yue, "A review of recent MOSFET threshold voltage extraction methods," *Microelectron. Rel.*, vol. 42, nos. 4–5, pp. 583–596, Apr./May 2002.

[31] X. Liu *et al.*, "Scanning probe nanopatterning and layer-by-layer thinning of black phosphorus," *Adv. Mater.*, vol. 29, no. 1, 2017, Art. no. 1604121.

[32] N. Haratipour, M. C. Robbins, and S. J. Koester, "Black phosphorus p-MOSFETs with 7-nm HfO_2 gate dielectric and low contact resistance," *IEEE Electron Device Lett.*, vol. 36, no. 4, pp. 411–413, Apr. 2015.

[33] Y. Huang *et al.*, "Interaction of black phosphorus with oxygen and water," *Chem. Mater.*, vol. 28, no. 22, pp. 8330–8339, 2016.

[34] G. Abellán *et al.*, "Fundamental insights into the degradation and stabilization of thin layer black phosphorus," *J. Amer. Chem. Soc.*, vol. 139, no. 30, pp. 10432–10440, 2017.

[35] J. Lu, J. Aarik, J. Sundqvist, K. Kukli, A. Hårsta, and J.-O. Carlsson, "Analytical TEM characterization of the interfacial layer between ALD HfO_2 film and silicon substrate," *J. Cryst. Growth*, vol. 273, nos. 3–4, pp. 510–514, 2005.

[36] K.-T. Lam, Z. Dong, and J. Guo, "Performance limits projection of black phosphorous field-effect transistors," *IEEE Electron Device Lett.*, vol. 35, no. 9, pp. 963–965, Jul. 2014.

[37] A. Prakash, H. Ilatikhameneh, P. Wu, and J. Appenzeller, "Understanding contact gating in Schottky barrier transistors from 2D channels," *Sci. Rep.*, vol. 7, Oct. 2017, Art. no. 12596.

[38] M. V. Fischetti, D. A. Neumayer, and E. A. Cartier, "Effective electron mobility in Si inversion layers in metal–oxide–semiconductor systems with a high-k insulator: The role of remote phonon scattering," *J. Appl. Phys.*, vol. 90, no. 9, pp. 4587–4608, 2001.

[39] X. Chen *et al.*, "High-quality sandwiched black phosphorus heterostructure and its quantum oscillations," *Nature Commun.*, vol. 6, Jun. 2015, Art. no. 7315.

[40] J. Na *et al.*, "Few-layer black phosphorus field-effect transistors with reduced current fluctuation," *ACS Nano*, vol. 8, no. 11, pp. 11753–11762, 2014.

[41] Y. Liu and P. P. Ruden, "Temperature-dependent anisotropic charge-carrier mobility limited by ionized impurity scattering in thin-layer black phosphorus," *Phys. Rev. B, Condens. Matter*, vol. 95, no. 16, 2017, Art. no. 165446.

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