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Ambipolar transport in van der Waals black arsenic field effect transistors

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Abstract

Black arsenic (BAs) is an elemental van der Waals semiconductor that is promising for a wide range of electronic and photonic applications. The narrow bandgap and symmetric band structure suggest that ambipolar (both *n*- and *p*-type) transport should be observable, however, only *p*-type transport has been experimentally studied to date. Here, we demonstrate and characterize ambipolar transport in exfoliated BAs field effect transistors. In the thickest flakes ($\sim$ 80 nm), maximum currents, I_{max}, up to 60 μA μm^{-1} and 90 μA μm^{-1} are achieved for hole and electron conduction, respectively. Room-temperature hole (electron) mobilities up to 150 cm^2 V^{-1} s^{-1} (175 cm^2 V^{-1} s^{-1}) were obtained, with temperature-dependence consistent with a phonon-scattering mechanism. The Schottky barrier height for Ni contacts to BAs was also extracted from the temperature-dependent measurements. I_{max} for both *n*- and *p*-type conductivity was found to decrease with reduced thickness, while the ratio of I_{max} to the minimum current, I_{min}, increased. In the thinnest flakes ($\sim$ 1.5 nm), only *p*-type conductivity was observed with the lowest value of $I_{min} = 400$ fA μm^{-1}. I_{max}/I_{min} ratios as high as 5×10^5 (5×10^2) were obtained, for *p*- (*n*-channel) devices. Finally, the ambipolarity was used to demonstrate a complementary logic inverter and a frequency doubling circuit.

Supplementary material for this article is available online

Keywords: Ambipolar, Black arsenic, Field effect transistor, Frequency doubler, Inverter

(Some figures may appear in colour only in the online journal)

1. Introduction

With scaling and performance of silicon-based transistors reaching their fundamental limits [1], a cross-disciplinary effort has gone into identification of novel material systems and device architectures that can outperform conventional solutions [2]. Van der Waals (vdW) semiconductors have recently gathered interest as post-silicon materials for use in conventional metal-oxide semiconductor field effect transistors (MOSFETs) [3–8] and tunneling FETs (TFETs) [9–13] because of their atomically smooth surfaces and extremely-thin body thicknesses that can lead to enhanced electrostatic gate control and improved scalability [6]. The most widely investigated vdW materials are the transition metal dichalcogenides (TMDs) [5–8, 14–17] which have been shown to enable sub-10 nm gate lengths [14], and ultra-low leakage currents [15], but can only achieve moderate drive currents due to their fairly low mobility and high effective mass [13]. TMDs also have stoichiometric defects [16] and only a few are suitable for use in complementary logic [17]. More recently, certain elemental vdW semiconductors such as black phosphorus (BP) [8, 18], silicene [19, 20] and tellurium [21], have gained interest for MOSFET applications due to their high mobility, thickness-dependent bandgap, and anisotropic carrier effective mass. Silicene has been used to fabricate MOSFETs which show similar transfer and output characteristics

as that of graphene devices [20], though its environmental instability and ultra-narrow bandgap make practical applications challenging. BP has been studied extensively for both MOSFETs [8, 18] and TFETs [9–12], but it also suffers from significant degradation in ambient atmosphere [22], and is difficult to thin down to single layers. Tellurium has been shown to be more stable than BP but is also difficult to thin and lacks good *n*-channel conductivity [21, 23].

Black arsenic (BAs) is an orthorhombic allotrope of arsenic which is isostructural to BP [24]. It has reduced reactivity to atmospheric oxygen and is more stable under ambient environmental conditions [25–27]. For example, Zhong, *et al* have shown that the relative degradation of MOSFET properties such as drive current and field effect mobility is less pronounced than that of BP [26]. In another work, Yun, *et al* showed that for a fixed period of time, oxygen-induced degradation in BAs under atmospheric conditions is much less than BP which degrades within hours of exposure to air [25]. Moreover, in dry-conditions, BAs layers been shown to have only 25% oxygen content after 60 days with no change to its underlying crystal structure. Figure 1(a) shows a three-dimensional (3D) rendered model of the crystal structure of BAs [28]. Each layer consists of two distinctive arsenic atoms and each atom forms covalent bonds with two in-plane and one out-of-plane neighbors making a non-planar structure. This crystal structure leads to a number of interesting properties in BAs, including highly anisotropic electrical and thermal transport properties along its two crystallographic directions (zigzag (ZZ) and armchair (AC)) [27], and a tunable direct bandgap. BAs therefore is a promising material for fabrication of various electronic [12], thermoelectric [27], and optical devices [29].

BAs is a particularly interesting material for high-performance electronic applications. Monolayer BAs MOSFETs have already been examined in simulations which have revealed excellent drive current performance [12, 30, 31]. Simulations performed using *ab-initio* methods have identified monolayer BAs as a future material for ultra-scaled MOSFETs, where sub-5 nm gate-length devices are predicted to meet ITRS (International Technology Roadmap for Semiconductors) requirements for high-performance and low-power applications [30, 31]. According to those calculations, the layer dependent bandgap of BAs varies from $\sim$ 0.2 eV (direct) in its bulk form to 0.73 eV (indirect) in its monolayer form [26]. The narrow bandgap and similar electron and hole effective masses suggest that symmetric ambipolar conduction should be possible, but to date, only *p*-type conductivity has been studied [26]. The ambipolar capability is particularly important for 2D material devices, where doping these materials to achieve p- and n-MOSFETs is not straightforward. In conventional complementary metal oxide semiconductor (CMOS) circuits, processes such as ion implantation are used to dope the MOSFETs [32]. However, doping in 2D materials using a method such as ion implantation will cause severe damage to their crystal structure [33], and other doping techniques are not well controlled [34, 35]. By electrostatically gating an ambipolar material, one can achieve both p-MOSFETs and n-MOSFETs without doping. As such, having an ambipolar material such as BAs can overcome the doping problem, and reduce the use of complicated fabrication techniques. Apart from the above applications, ambipolar transport can also be used to design non-volatile memory [36] with a broad window of operation and to create powerful bipolar catalysts that can control two sets of reactions, anodic and cathodic using just one material [37]. Here, we demonstrate ambipolar BAs MOSFETs, and characterize their properties as a function of bias, thickness, and temperature. The devices, which utilize Ni contacts, show strong ambipolar behavior for thick flakes, but with decreasing thickness, the devices exhibit less *n*-type behavior. The minimum current at the ambipolar point decreases in thinner flakes, consistent with a thickness-dependent bandgap. Temperature-dependent measurements suggest that the Fermi level is slightly on the valence-band side of the mid-gap position, and the results can be used to extract the Schottky barrier height and approximate bandgap of thick BAs. Finally, the ambipolar functionality is utilized to demonstrate two practical applications: (1) a complementary logic inverter, where the inherent ambipolarity of BAs is used to achieve p-MOSFETs and n-MOSFETs by tuning the applied electric field onto the gate terminal, and (2) a frequency doubler, where the BAs MOSFET is biased at the ambipolar point (the point of minimum conductance) to double the frequency of an input analog signal.

2. Results and discussion

BAs flakes were mechanically exfoliated from a bulk crystal (purchased from a commercial vendor—2D Semiconductors, USA) using the Scotch tape method and transferred onto SiO_2/Si substrates. Figure 1(b) shows an atomic force microscopy (AFM) image of a typical multi-layer exfoliated BAs flake. A line scan on the AFM image shows the thickness of the flake as 10 nm. The orthorhombic crystal structure of BAs was confirmed by performing Raman spectroscopy. Three Raman modes (shown in figure 1(c)): $A^1{}_g \sim 220.1$ cm^{-1}, $B_2{}_g \sim 226.3$ cm^{-1}, and $A^2{}_g \sim 253.6$ cm^{-1} were identified which are in close agreement with the previously reported data [38, 39]. Angle-resolved polarized Raman spectroscopy was performed on the BAs flakes to further establish the presence of anisotropy in the crystal lattice. Linearly polarized light (in the *x*-*y* plane) was focused on the flake and the polarization angle was rotated. It was revealed that the intensity of the Raman modes changed with change in the polarization angle relative to the crystal. Figure S1(a) (supporting information (available online at stacks.iop.org/NANO/31/405203/mmedia)) shows the Raman spectra of the BAs flake for different angles of polarization. The change in peak intensities with change in polarization of incident light for the modes $A^1{}_g$ at 220.1 cm^{-1} (figure 1(d)) and $A^2{}_g$ at 253.6 cm^{-1} (figure S1(b)) were plotted onto polar plots which revealed two-fold symmetries for them. The angular position at maximum and minimum intensities corresponded to crystal orientations at AC and ZZ, respectively. Figure 1(e) shows a plan-view high-angle annular dark-field (HAADF)-scanning transmission electron microscopy (STEM) image of an exfoliated BAs

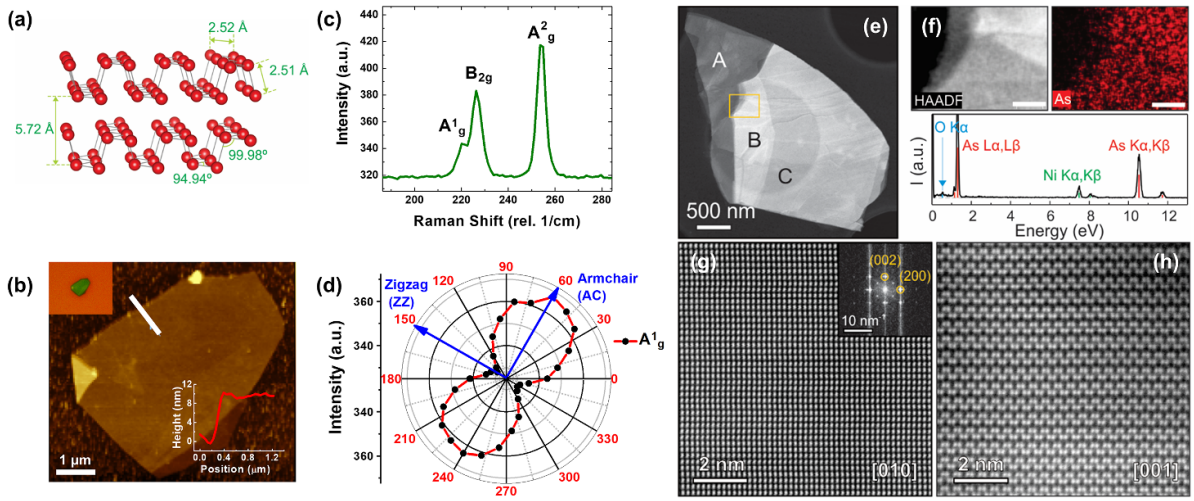

Figure 1. (a) 3D rendered structure of a bilayer BAs. (b) AFM micrograph of one of the exfoliated flakes on SiO_2/Si substrate. Inset: Top Left: Optical micrograph of the same flake; Bottom Right: AFM line-scan along the white solid line. (c) Raman spectrum of an exfoliated flake showing three modes $A^1{}_g$, $A^2{}_g$ and $B_2{}_g$ under excitation. (d) Polar plot of the Raman intensity of the mode $A^1{}_g$ with respect to polarization angle of incident light. (e) Plan-view HAADF-STEM image of a BAs flake having thinner and thicker (brighter) regions on a support holey-carbon film of a TEM grid (f) Top left: HAADF-STEM image (scale bar: 100 nm) of the highlighted area (yellow box) shown in (e). Top right: EDX map of the flake showing arsenic signal. Bottom: EDX spectrum demonstrating dominant As, with weak Ni and O signal. (g) Atomic resolution HAADF-STEM plan-view image of the BAs flake shown in (e) with the fast Fourier transform of the image in the inset. (h) Cross-sectional HAADF-STEM image of a BAs flake viewed along the armchair direction. Individual layers separated by vdW gap are visible.

flake. Thickness of the flake was estimated using the electron energy-loss spectroscopy log-ratio method [40], and the thickness of the regions A, B, and C in figure 1(e) were estimated to be $\sim$ 10, $\sim$ 35, and $\sim$ 20 nm, respectively. Chemical composition of the flake was analyzed using energy dispersive x-ray (EDX) spectroscopy in STEM (figure 1(f)). Strong As signal from the flake was observed. The EDX spectrum from the spatial map shows peaks from As, O, and Ni (from the TEM grid) and no other elements. Quantitative analysis of the EDX spectrum yields, 98.1 at% of As and 1.9 at% of O (Ni peaks are excluded), indicating practically pure BAs. Figure 1(g) shows atomic-resolution HAADF-STEM image of BAs in the plan-view ([010]) with fast Fourier transform (FFT) of the image in the inset suggesting orthorhombic crystal structure. A cross-sectional atomic-resolution HAADF-STEM image in the [001] direction (figure 1(h)) shows the characteristic atomic configuration along the armchair direction, reaffirming the crystal structure of BAs.

To fabricate the MOSFETs, BAs flakes were first exfoliated using adhesive tape and transferred onto 300 nm of SiO_2 thermally grown over an n^+ Si substrate. Electron-beam lithography was used to pattern the substrates followed by electron-beam deposition and lift-off of Ni/Au to define the source/drain electrodes. Ni was chosen as the contact metal as it has successfully been used as a contact material for studying ambipolar transport in BP transistors (supporting information, section 9) [41]. In that work, it was observed that the Fermi level was aligned near the middle of the bandgap allowing ambipolar transport. In another work, Anugrah, *et al* showed ambipolar transport using permalloy (an alloy consisting of 80% nickel and 20% iron) contacts to BP [42]. Figure 2(a) shows a schematic of a completed BAs globally back-gated MOSFET and figure 2(b) shows the height AFM micrograph of one of the fabricated MOSFETs with 8.7-nm-thick BAs channel. Several BAs MOSFETs were fabricated with varying channel thicknesses and AFM was performed to determine the thicknesses of the flakes which varied from 1.5 nm to 80 nm. Table S1 (supporting information, section 2) shows the summary of the physical dimensions (channel thickness, t_{BAs}, effective channel length, L, and channel width, W) for a total of 34 devices. Figure 2(c) shows the transfer characteristics (drain current, I_D, vs. gate voltage, V_G) of 5 BAs MOSFETs with varying channel thicknesses. It can be clearly seen that thicker flakes show more ambipolar conduction than thinner flakes. The thickest of the flakes ($t_{BAs} = 13.0$ nm) shows a very symmetric transition from hole to electron conduction as the gate voltage is swept from negative to positive, while the n-type arm is completely absent in the device with the thinnest channel thickness ($t_{BAs} = 1.5$ nm). This result is indicative of a Fermi level that is aligned near mid-gap in thick flakes, but more towards the valence band edge in thinner flakes. Band diagrams showing the qualitative Fermi level position in thick- and thin-channel BAs MOSFETs are provided in Section 10 of the Supporting Information. Figure 2(d) shows the minimum current, I_{min}, plotted vs. channel thickness. The decrease of I_{min} in thinner flakes is indicative of a thickness-dependent bandgap, consistent with results for BP [8] as well as results for p-channel BAs MOSFETs [26]. The lowest I_{min} recorded was $\sim$ 400 fA μm^{-1}($t_{BAs} = 1.5$ nm), which is at the noise floor of our measurement setup. Thinner flakes have a larger bandgap than thicker flakes allowing thin-channel MOSFETs to have lower minimum current than the thicker-channel devices. The same inference can be derived from figure 2(e) where we

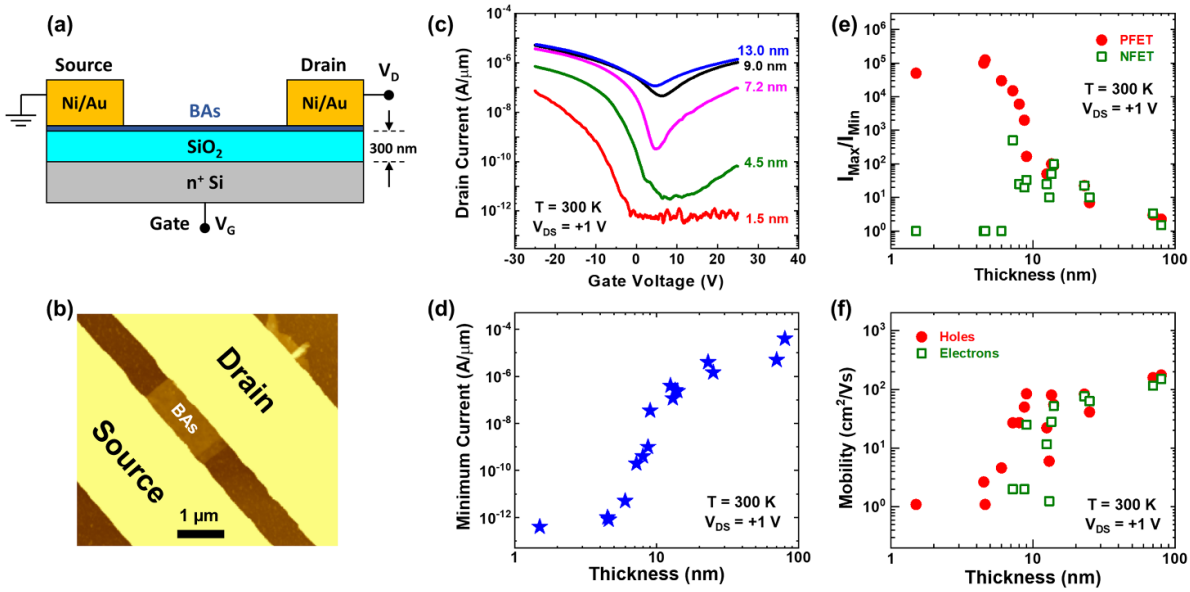

Figure 2. (a) Schematic of the as-fabricated BAs FET with a global SiO_2/Si back gate. (b) AFM micrograph of one of the fabricated FETs with 8.7 nm thick BAs channel. (c) Transfer (I_D vs. V_G) characteristics of 5 BAs FETs having different channel thicknesses (d)–(f) Dependence of (d) I_{min}, (e) I_{max}/I_{min} and (f) mobility, on various channel thicknesses for both electron and hole conduction.

see an increase in I_{max}/I_{min} ratio with decreasing thickness down to $\sim$ 5 nm flakes, at which point further improvement is limited by the noise floor. The highest I_{max}/I_{min} ratio for *p*-channel (*n*-channel) conduction was 5×10^5 for $t_{BAs} = 4.5$ nm (5×10^2 for $t_{BAs} = 7.2$ nm) based upon a gate voltage range between $\pm$ 25 V. We believe that *p*-channel conductivity dominates in thinner flakes primarily due to the high work function of Ni which places the Fermi level below mid-gap in BAs, combined with the thickness-dependent bandgap, which increases the asymmetry of the Ni/BAs as the flake gets thinner. We do note that a higher I_{max} on the *n*-channel side could occur if a more positive gate voltage had been applied.

The field effect mobility, μ, of our devices was calculated by using the equation:

$$\mu = \frac{L}{W}\frac{d}{V_{DS}\varepsilon_r\varepsilon_o}g_m, \tag{1}$$

where L is the channel length defined by the distance between the source and drain electrodes, W is the channel width, ε_0 is the permittivity of free space, $\varepsilon_r = 3.9$ is the relative dielectric constant for SiO_2, $d = 300$ nm is the thickness of SiO_2, V_{DS} is the drain-to-source voltage, and g_m is the transconductance obtained from the derivative of the I_D-V_G curve. Figure 2(f) shows μ vs. t_{BAs} plots for electrons and holes. An increase in the mobility was observed with increase in the thickness of the sample. For the thickest samples (80 nm), mobility values as high as 150 $cm^2\ V^{-1}\ s^{-1}$ (holes) and 175 $cm^2\ V^{-1}\ s^{-1}$ (electrons) were observed. The mobility values for thick flakes are significantly higher than those found in ref. [25], a result which we attribute to the low contact resistance in our samples, even in the thickest flakes. Unlike the results in ref. [25], we did not observe degradation of the contact resistance as a result of out-of-plane interlayer transport, as has been reported for BP [43] and MoS_2 [44]. Since the crystal orientation of the flakes relative to the transport direction was not controlled in this experiment, the mobility distribution for both holes and electrons has some degree of variability.

To gain additional insight into the transport properties in BAs, temperature-dependent transfer characteristics were also taken for one of the thicker flakes ($t_{BAs} = 11$ nm). Figure 3(a) shows the I_D-V_G characteristics of a multilayer BAs MOSFET for various temperatures varying from 100 K to 360 K. The value of I_{max}/I_{min} increases with decreasing temperature for both the *p*- and *n*-channel sides. At large positive or negative V_G, for both electron and hole conduction, hardly any change in I_{max} is observed. This is due to the fact that at such large gate voltage biases the contacts become transparent to the carriers and injection into the channel is no longer dominated by thermionic emission. Hence, the Schottky barrier height can only be extracted when the device is operating in the subthreshold regime. The temperature-dependence of the drain current can be understood by using the thermionic emission equation:

$$I_D = A^* T^2 exp\left[-\frac{1}{k_B T}\left(\Phi_{SB} - \frac{qV_{DS}}{\eta}\right)\right], \tag{2}$$

where A^* is the effective Richardson constant (in A K^{-2}), T is the temperature (in K), k_B is Boltzmann's constant (in eV/K), Φ_{SB} is the effective Schottky barrier height (in eV), q is the electronic charge (in units of the electronic charge, e), V_{DS} is the applied voltage between drain and source terminals (in V), and η is an empirically-determined ideality factor. The activation energy in the above equation is given by the term $\Phi_{SB} - \frac{qV_{DS}}{\eta}$ where the term $\frac{qV_{DS}}{\eta}$ tells us the degree by which the energy barrier is lowered by the application of the source-drain voltage. Arrhenius plots ($\ln(I_D/T^2)$ vs $1/k_BT$) are made for each gate voltage for different V_{DS} values and then the slope ($\Phi_{SB} - \frac{qV_{DS}}{\eta}$) is obtained. The slope is then plotted

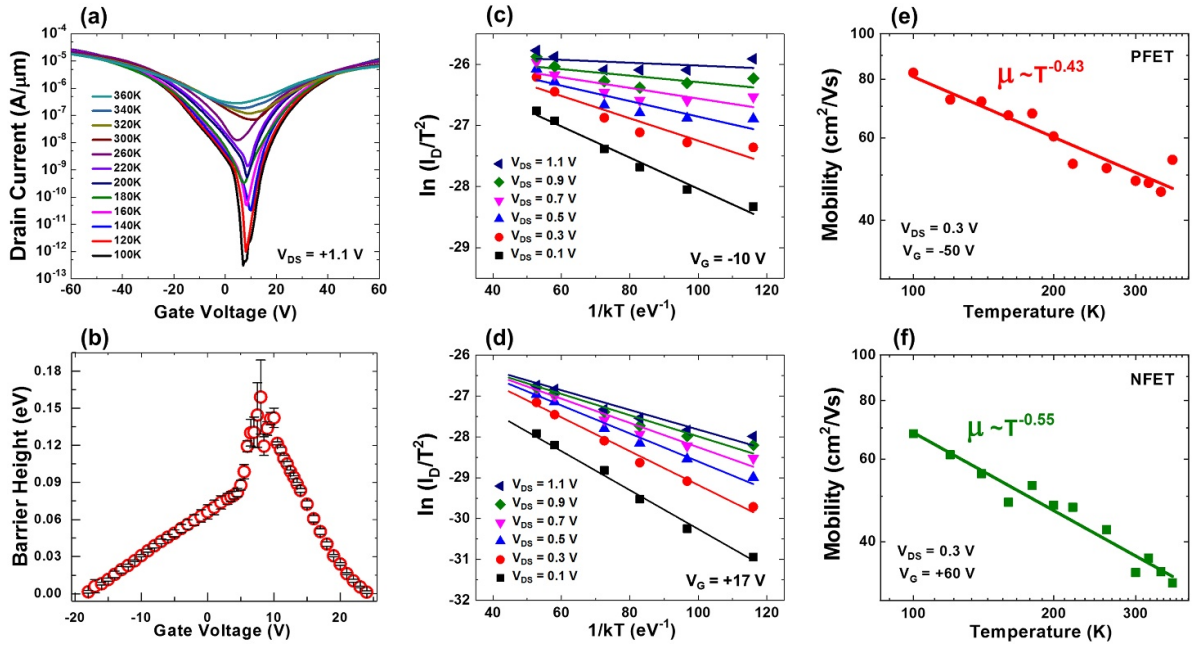

Figure 3. Temperature-dependent characteristics for a BAs MOSFET with 11 nm thick channel. (a) Temperature-dependent ambipolar transfer (I_D vs. V_G) characteristics. (b) Schottky barrier height as a function of gate bias voltage. (c)-(d) Arrhenius plots for different source-drain biases at gate voltages of (c) $V_G = -10$ V and (d) $V_G = +17$ V. (e)-(f) Mobility vs temperature plot (e) *p*-channel and (f) *n*-channel conduction with fitting parameters of power law given by $\mu \propto T^{-\lambda}$.

against V_{DS}, and the resulting curve, when extrapolated linearly to $V_{DS} = 0$ V, yields Φ_{SB}. The extracted value of Φ_{SB} is plotted vs. V_G in figure 3(b). Figures 3(c) and (d) show representative Arrhenius plots at two gate voltages, $V_G = -10$ V and $V_G = +17$ V, respectively, where the former corresponds to hole conduction while the latter represents electron conduction. From these plots, it can be easily seen that the slopes are linear and negative, which indicates a positive activation energy, and thus, thermally activated transport. The slopes from Arrhenius plots in figures 3(c) and (d) are plotted against V_{DS} in figures S2(a) and S2(b), respectively. The process was repeated for all the gate voltages, and Φ_{SB} was extracted and plotted against V_G as shown in figure 3(b). The barrier height reaches a peak at 0.14 eV, approximately at the gate voltage corresponding to minimum conduction. At the point of minimum conduction, I_{min} has an equal contribution of electron injection from the drain side and hole injection from the source terminal [8]. Hence, it is reasonable to conclude that $0.14\,\text{eV} = E_G/2$, and so $E_G = 0.28$ eV for the 11-nm-thick BAs flake. We note that this estimation method is reasonably valid for thick flakes with relatively symmetric ambipolar characteristics, but such an extraction for thinner flakes requires more detailed modeling. It is important to note that previous studies [45, 46] have shown that interactions can take place between the deposited metal and the semiconductor even at low temperatures which can affect the band alignments and Fermi-level pinning. Therefore, further study of the precise details of the metal/BAs interface is warranted in the future. Figures 3(e) and (f) show the temperature dependence of μ from $T = 100$ K to 360 K. Both the hole and electron mobilities increase with decreasing temperature. An exponential fit based upon the power law, $\mu \propto T^{-\lambda}$, revealed $\lambda = 0.43$ and 0.55 for holes and electrons, respectively at $V_{DS} = 0.3$ V. This result indicates that the mobility in the ambipolar BAs FETs is primarily phonon-limited for both holes and electrons. Once again, this result differs from that in ref. [25] (for holes), as we did not observe evidence of strong ionized impurity scattering. The value of λ obtained for BAs is comparable to that of BP [47], but is much lower compared to traditional semiconductors such as Si [48], and Ge [49], as well as other 2D materials such as MoS_2 [50].

Figures 4(a) and (b) show the output characteristics (I_D vs. V_{DS}) for *p*- and *n*-channel MOSFETs respectively made from two different BAs flakes. The devices show relatively linear characteristics, indicative of Ohmic contacts, and the contacts remain relatively linear for all temperatures tested (figure S3). Figure 4(c) shows the circuit diagram and the schematic of a BAs inverter fabricated used these same two flakes. The DC input-output characteristics of the inverter (figure 4(d)) can be divided into five different regions; Region-I shows high output voltage (corresponding to low V_{in}), region III has low output signal (corresponding to high V_{in}) and region II is where the transition happens. The maximum gain obtained by our BAs inverter is 0.25, though such a low value is mainly attributed to the very thick gate dielectric of 300 nm, as well as the low V_{DD} value used such that the devices operate in the linear regime. It should also be noted that in region IV (V), V_{out} starts decreasing (increasing) again as V_{in} is made more negative (positive). This behavior arises due to 'overly' ambipolar behavior of these relatively thick BAs devices, and shows that fine-tuning of the threshold voltage and off-state leakage is important to optimize such devices for use in realistic logic circuits. To provide more controllability over the inverter, local back-gate electrodes could be utilized to provide separate gates

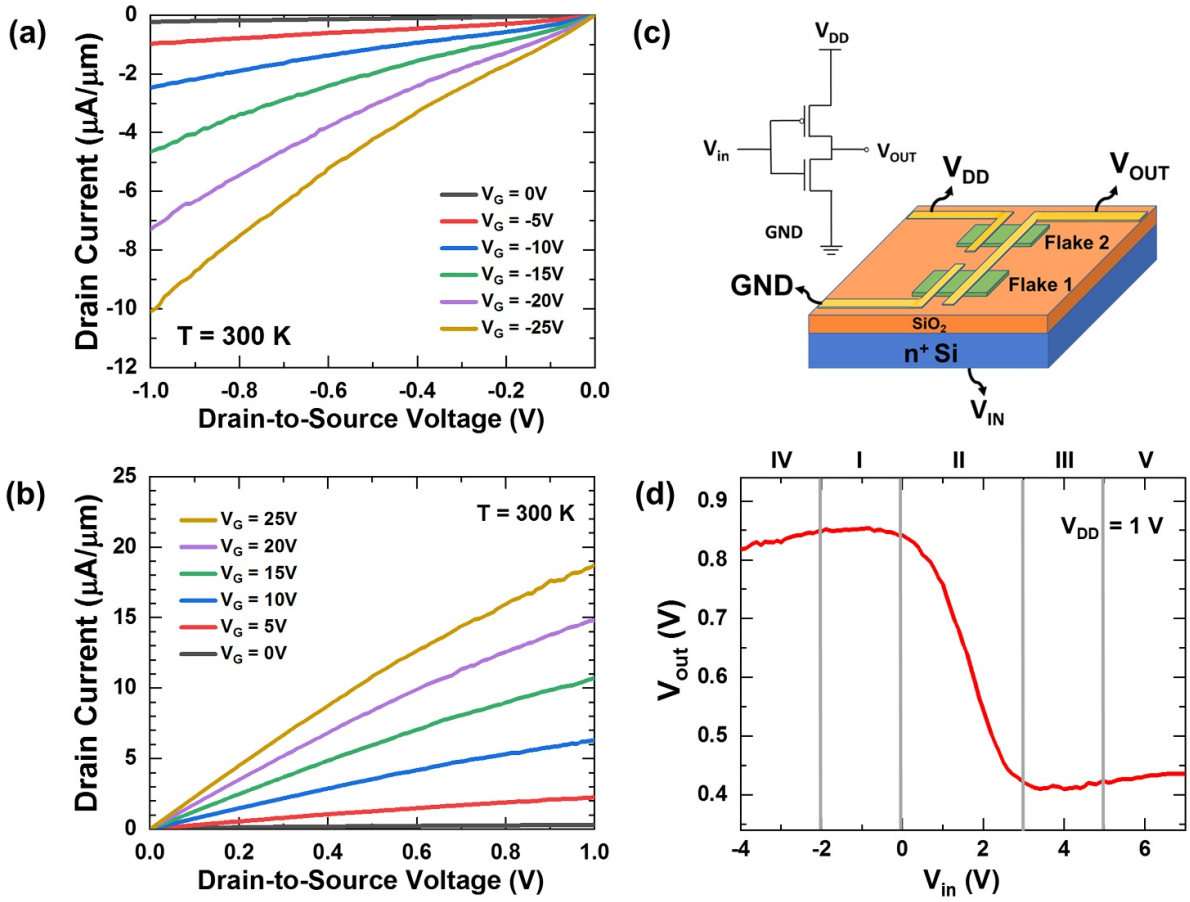

Figure 4. (a)-(b) Output (I_D vs. V_{DS}) characteristics of the BAs FET biased as (a) *p*-channel MOSFET (Flake 2) and (b) *n*-channel MOSFET (Flake 1). (c) Circuit diagram and schematic of the as-fabricated inverter. (d) Input-output characteristics of the inverter in (c).

to each MOSFET in the inverter so that the threshold voltage of each device can be controlled independently. Nevertheless, this work provides a baseline demonstration of logic operations in ambipolar BAs where significant further optimization is possible.

As a final demonstration of the ambipolar operation of BAs transistors, locally back-gated devices were fabricated. Here, a process similar to that reported in reference [8] was used, where a Ti/Pd local gate electrode was fabricated on a Si/SiO_2 substrate and then atomic layer deposition was used to deposit 10 nm of HfO_2. Then, a BAs flake was positioned and exfoliated above the gate region followed by Ni/Au source-drain electrodes (see Experimental Section for the fabrication process). A schematic of the completed locally back-gated device is shown in figure 5(a). Figure 5(b) shows the I_D vs. V_G characteristic of the locally back-gated device. Clearly, the small equivalent oxide thickness (∼2.5 nm) of HfO_2 reduced the gate voltage swing required to modulate drain current. The device shows very symmetric ambipolar behavior with high current drive in both the electron and hole branches. The transconductance values are shown in figure 5(c) where a peak g_m of 45 μS/μm (36 μS/μm) is observed for the *p*-channel (*n*-channel) branch, once again showing excellent symmetry between electron and hole transport.

To highlight the analog circuit potential of ambipolar BAs FETs, we demonstrate the operation of the device as a frequency doubler. If the BAs ambipolar FET is biased at the point of minimum conduction with an input sinusoidal signal of frequency, *f*, a rectified waveform of frequency 2 *f* can be obtained at the drain terminal, as shown in the inset of figure 5(d). Single FET based frequency multipliers in particular have a great advantage over analog CMOS based architectures due to reduced transistor count and absence of any device matching requirement [51]. Recently, graphene FETs have been used as frequency multipliers [52, 53], however, graphene has the disadvantage that it is not well-suited to perform other functions such as high on-off-ratio devices for logic operations. On the other hand, the variable bandgap of BAs makes it attractive to produce multi-functional devices where the channel thickness can be optimized for the application under consideration. The frequency doubling performance of our locally back-gated BAs FET is shown in figure 5(d). Here, an input sinusoidal signal of $f = 100$ Hz with an appropriate DC offset was applied such that the input signal was biased near the point of minimum conduction. The resultant output signals have dominant frequencies of 200 Hz, with total harmonic distortion (THD) of 13.5% and 30.2% for $V_{DD} = 0.2$ V and 0.7 V, respectively. Clearly the second harmonic (200 Hz) signal is the dominant frequency in the output

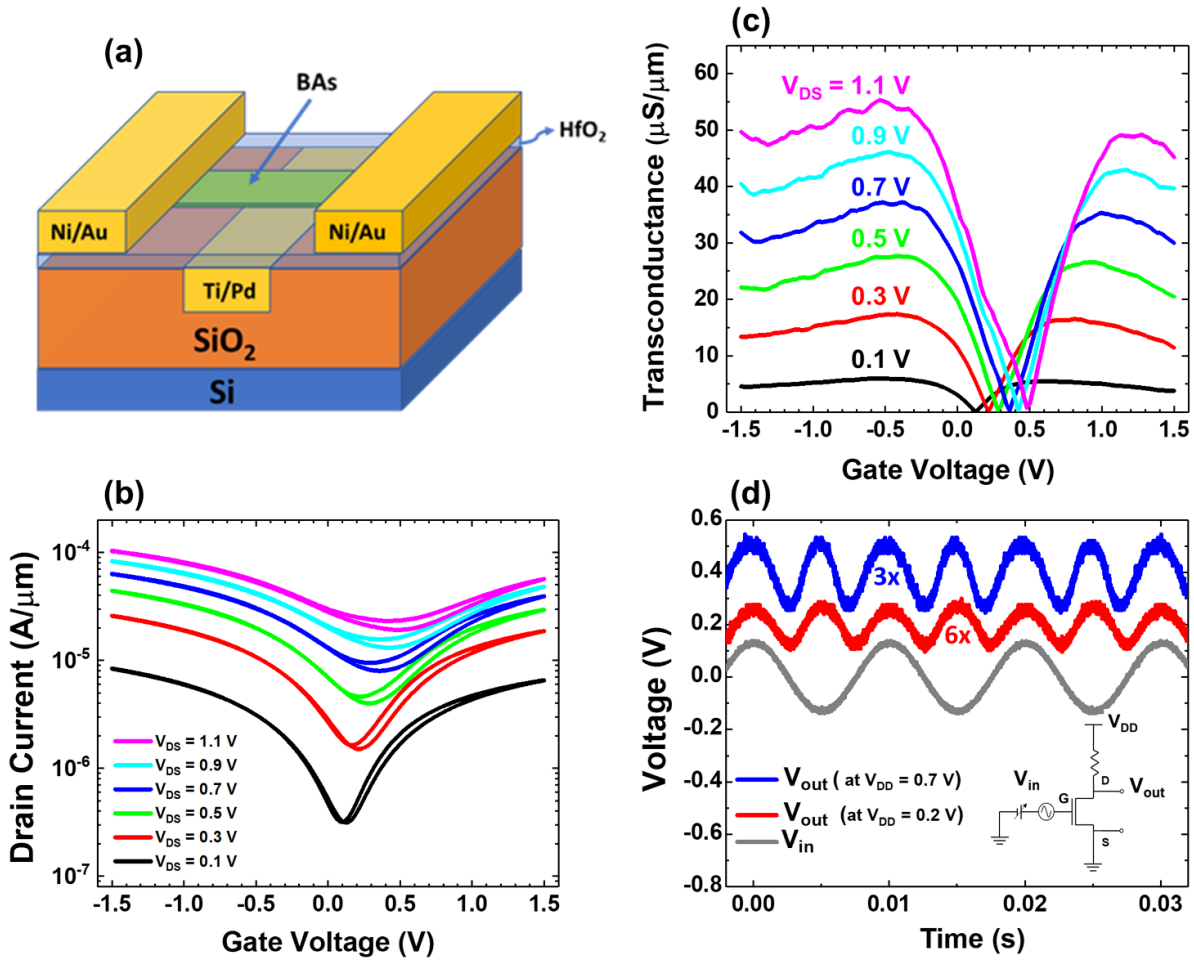

Figure 5. (a) Schematic diagram of locally back-gated BAs MOSFET with HfO_2 gate dielectric. (b) Transfer (I_D vs. V_G) characteristics of the BAs FET with local backgate for various values of V_{DS}. (c) Transconductance vs gate voltage of the BAs FET on a locally back-gated structure for various values of V_{DS}. (d) AC component of input signal for $V_{DS} = +0.2$ V (grey) and output signals for $V_{DD} = +0.2$ V (red) and $V_{DD} = +0.7$ V (blue) from the frequency doubler. Due to slightly different phase shifts in the output waveforms relative to the input, the output characteristics for $V_{DD} = +0.2$ V and $+0.7$ V have been offset on the x-axis for visual clarity. These curves have also been shifted on the y-axis, again for graphical clarity. The time scales of the output characteristics have been shifted slightly, and the red and blue curves have been offset on the voltage axis, for graphical clarity. Inset: circuit diagram of a single-FET frequency doubler.

signals for all V_{DD} values (figure S4 and table S2 in the supporting information provide additional data). Further improvement in the speed of the doublers is possible by measuring using high-speed probes and utilizing an optimized, multi-finger geometry to minimize parasitic resistances. THD values can readily be improved by optimizing the load condition, DC offset and contact metal.

3. Conclusion

In summary, we have successfully fabricated ambipolar FETs using a highly pure BAs crystal. Owing to its reduced oxygen-induced degradation in ambient environmental conditions, BAs offers a promising alternative to the less-stable BP for high-performance electronic devices. In this work, the fabricated black arsenic ambipolar FETs showed high mobility values, highly symmetric drive currents and low current at the minimum conduction state both for electrons and holes. The electron and hole mobility were determined as a function of temperature, and the low-temperature device characteristics helped us to determine the Schottky barrier height present at the Ni/BAs interface. Lastly, we made use of the symmetric ambipolar behavior of BAs to fabricate a complementary logic inverter using substrate-gated devices, and a frequency double using a locally back-gated device geometry. The above results are an important first step in characterizing the properties of this promising van der Waals materials for analog and digital nanoscale device applications. Additional controlled, side-by-side, experiments comparing BAs to BP will be useful to understand the ultimate stability and performance advantages of BAs, and will be important to further assess the future outlook for BAs electronic devices.

4. Experimental section

STEM sample preparation for plan-view imaging: BAs flakes were first mechanically exfoliated using the standard Scotch tape method and transferred onto a SiO_2/Si substrate.

The flakes were spin coated with 500 nm thick polymethyl methacrylate (950 PMMA C4) and then a soft bake was performed at 120 °C for 2 min. A wet transfer method was used to transfer the flakes from the SiO_2 substrate to the TEM grid. Using a sharp knife, the spin coated PMMA was removed from the edges of the substrate and then the substrate was made to float on a 10:1 buffered oxide etch (BOE) solution. BOE solution starts entering below PMMA to etch SiO_2 beneath it and after 20 min all of SiO_2 was etched away. This caused the PMMA flake to float on the BOE solution while the remainder of the Si substrate sank down to the bottom of the BOE. The floating PMMA/BAs stack was transferred to DI water to clean the residual BOE. The stack was then transferred to a TEM grid (Quantifoil Ni TEM grid with holey carbon support, 658–300-NI. Hole Size = 1.2 μm) and washed off in acetone to remove PMMA, with the BAs attached to the TEM grid.

STEM sample preparation for cross-sectional imaging: The samples for cross-sectional TEM were prepared by a focused ion-beam (FIB) lift-out method using a FEI Helios Nanolab G4 dual-beam FIB. First, the BAs flakes were mechanically exfoliated using the standard Scotch tape method and transferred onto a SiO_2/Si substrate having identification marks over it. With the help of these identification marks, the flake of interest was located under the SEM. Then, a cross-sectional lamella was cut out from the specimen using a 30 kV Ga-ion beam and polished using a 2 kV Ga-ion beam to remove the surface damage from the FIB procedure.

STEM characterization: STEM experiments were carried out using aberration-corrected FEI Titan G2 60–300 STEM equipped with a CEOS DCOR probe corrector and super-X energy dispersive x-ray (EDX) spectrometer. The microscope was operated at 200 kV and a beam current was adjusted to be $\sim$ 30 pA. The probe convergence angle was 17.2 mrad and annular dark-field (ADF) detector inner and outer angles for HAADF-STEM images were 55 and 200 mrad. Ar plasma cleaning of a TEM specimen was carried out for $\sim$ 7 s before each experiment.

Experimental Raman spectra of BAs: Thin mechanically exfoliated BAs flakes were analyzed using a Witec Alpha 300 R confocal Raman microscope with UHTS300 spectrometer and DV401 CCD detector. Flakes were irradiated with a 532 nm Nd:YAG laser with a spot size of 0.5 μm.

AFM scan of exfoliated BAs flake: Before performing the AFM scan, the flake was passivated with evaporated aluminum oxide (20 nm) to avoid degradation in air. Bruker Nanoscope V Multimode 8 SPM (Scanning Probe Microscope) in peak force QNM (Quantum Nano Mechanical) tapping mode was used to perform the AFM scan. Gwyddion software was then used to analyze the scanned image (Resolution: 256 $\times$ 256 pixels).

Fabrication procedure for locally back-gated FETs: All patterning steps were performed using electron-beam lithography (EBL) followed by developing in a 3:1 solution of isopropyl alcohol: methyl isobutyl ketone while electron-beam evaporation was used for all metallization steps. Highly doped *n*-type Si with 300 nm of thermally grown SiO_2 were used as the starting substrates. The process began with patterning and developing of the local gate electrode. EBL was performed to pattern the gate region, followed by recessing the SiO_2 by 40 nm using reactive ion etching in CHF_3/CF_4/Ar and another 10 nm using etch using 10:1 BOE. Next, Ti/Pd (5 nm/20 nm) was evaporated and lifted off to create the local backgate. Atomic layer deposition (ALD) was used to deposit 10 nm of HfO_2 gate dielectric over the gate electrode where water vapor and tetrakis(dimethylamido)-hafnium(IV) were used as the ALD precursors. BAs flakes were then exfoliated onto PDMS, aligned, and transferred to the local backgates using a transfer stage. Finally, source and drain electrodes consisting of Ni/Au (20 nm/50 nm) were patterned and lifted off.

Electrical characterization of BAs MOSFETs: Post fabrication, BAs MOSFET devices were loaded inside a Lakeshore CPX-VF cryogenic probe station. The station was pumped down until a the pressure of 2×10^{-6} Torr was reached. Semiconductor parameter analyzer (Keysight B1500 A) was used to perform all the electrical measurements. No thermal annealing was performed on the fabricated devices.

Supporting information

Angle resolved Raman spectroscopy on BAs flakes, table showing thickness dependent transport properties, Arrhenius plot slope vs. drain-to-source voltage plots, output characteristics of BAs MOSFETs at different temperatures and total harmonic distortion calculation.

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Conflict of interest

The authors declare no competing financial interest.

Contributions

P.G. and S.J.K. designed and directed this study and analyzed the results. P.G. performed device fabrication. P.G., J.W. and S.J.K. performed process development. P.G. and S.J.K. performed device characterization. H.Y., S.G. and A.M performed TEM characterization. P.G. and S.J.K. wrote the manuscript. The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

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References

[1] Keyes R W 2001 Fundamental limits of silicon technology *Proc. IEEE* **89** 227–39
[2] Nikonov D E and Young I A 2015 Benchmarking of beyond-CMOS exploratory devices for logic integrated circuits *IEEE J. Explor. Solid-State Comp. Dev. Circ.* **1** 3–11
[3] Fiori G, Bonaccorso F, Iannaccone G, Palacios T, Neumaier D, Seabaugh A, Banerjee S K and Colombo L 2014 Electronics based on two-dimensional materials *Nat. Nanotechnol.* **9** 768–79
[4] Alam K and Lake R K 2012 Monolayer MoS_2 transistors beyond the technology road map *IEEE Trans. Elect. Dev.* **59** 3250–4
[5] Schwierz F, Pezoldt J and Granzner R 2015 Two-dimensional materials and their prospects in transistor electronics *Nanoscale* **7** 8261–83
[6] Chhowalla M, Jena D and Zhang H 2016 Two-dimensional semiconductors for transistors *Nature Rev. Mater.* **1** 16052
[7] Ma R *et al* 2019 $MoTe_2$ lateral homojunction field-effect transistors fabricated using flux-controlled phase engineering *ACS Nano* **13** 8035–46
[8] Haratipour N, Namgung S, Oh S-H and Koester S J 2016 Fundamental limits on the subthreshold slope in Schottky source/drain black phosphorus field-effect transistors *ACS Nano* **10** 3791–800
[9] Wu P, Ameen T, Zhang H, Bendersky L A, Ilatikhameneh H, Klimeck G, Rahman R, Davydov A V and Appenzeller J 2019 Complementary black phosphorus tunneling field-effect transistors *ACS Nano* **13** 1377–85
[10] Robbins M C and Koester S J 2017 Crystal-oriented black phosphorus TFETs with strong band-to-band-tunneling anisotropy and subthreshold slope nearing the thermionic limit *Int. Electron Devices Meeting (IEDM), San Francisco, CA* (https://doi.org/10.1109/IEDM.2017.8268399)
[11] Robbins M C, Golani P and Koester S J 2019 Right-angle black phosphorus tunneling field effect transistor *IEEE Elect. Dev. Lett.* **40** 1988–91
[12] Szabó Á, Klinkert C, Campi D, Stieger C, Marzari N and Luisier M 2018 Ab Initio simulation of band-to-band tunneling FETs with single- and few-layer 2-D materials as channel *IEEE Trans. Elect. Dev.* **65** 4180–7
[13] Szabó Á, Koester S J and Luisier M 2015 Ab-initio simulation of van der Waals $MoTe_2$–SnS_2 heterotunneling FETs for low-power electronics *IEEE Elect. Dev. Lett.* **36** 514–6
[14] Desai S B *et al* 2016 MoS_2 transistors with 1 nanometer gate lengths *Science* **354** 99–102
[15] Kshirsagar C U, Xu W, Su Y, Robbins M C, Kim C H and Koester S J 2016 Dynamic memory cells using MoS_2 field-effect transistors demonstrating femtoampere leakage currents *ACS Nano* **10** 8457–64
[16] Yu Z, Ong Z Y, Li S, Xu J B, Zhang G, Zhang Y W, Shi Y and Wang X 2017 Analyzing the carrier mobility in transition metal dichalcogenide MoS_2 field effect transistors *Adv. Funct. Mater.* **27** 1604093
[17] Cho A-J, Park K C and Kwon J Y 2015 A high-performance complementary inverter based on transition metal dichalcogenide field-effect transistors *Nanoscale Res. Lett.* **10** 115
[18] Haratipour N, Liu Y, Wu R J, Namgung S, Ruden P P, Mkhoyan K A, Oh S-H and Koester S J 2018 Mobility anisotropy in black phosphorus MOSFETs with HfO_2 gate dielectrics *IEEE Trans. Elect. Dev.* **65** 4093–101
[19] Lew Yan Voon L C, Zhu J and Schwingenschlögl U 2016 Silicene: recent theoretical advances *Appl. Phys. Rev.* **3** 040802
[20] Tao L, Cinquanta E, Chiappe D, Grazianetti C, Fanciulli M, Dubey M, Molle A and Akinwande D 2015 Silicene field-effect transistors operating at room temperature *Nat. Nanotech.* **10** 227–31
[21] Ren X, Wang Y, Xie Z, Xue F, Leighton C and Frisbie C D 2019 Gate-tuned insulator-metal transition in electrolyte-gated transistors based on tellurene *Nano Lett.* **19** 4738–44
[22] Huang Y *et al* 2016 Interaction of black phosphorus with oxygen and water *Chem. Mater.* **28** 8330–9
[23] Zhou G *et al* 2018 High-mobility helical tellurium field-effect transistors enabled by transfer-free low-temperature direct growth *Adv. Mater.* **30** 1803109
[24] Seidl M, Balázs G and Scheer M 2019 The chemistry of yellow arsenic *Chem. Rev.* **119** 8406–34
[25] Yun H, Ghosh S, Golani P, Koester S J and Mkhoyan K A 2020 Layer-dependence of dielectric response and water-enhanced ambient degradation of highly-anisotropic black as *ACS Nano* **14** 5988–97
[26] Zhong M, Xia Q, Pan L, Liu Y, Chen Y, Deng H X, Li J and Wei Z 2018 Thickness-dependent carrier transport characteristics of a new 2D elemental semiconductor: black arsenic *Adv. Funct. Mater.* **28** 1802581
[27] Chen Y B *et al* 2018 Black arsenic: a layered semiconductor with extreme in-plane anisotropy *Adv. Mater.* **30** 1800754
[28] Jain A *et al* 2013 The materials project: a materials genome approach to accelerating materials innovation *APL Mater.* **1** 011002
[29] Long M *et al* 2017 Room temperature high-detectivity mid-infrared photodetectors based on black arsenic phosphorus *Sci. Adv.* **3** e1700589
[30] Sun X, Song Z, Liu S, Wang Y, Li Y, Wang W and Lu J 2018 Sub-5 nm monolayer arsenene and antimonene transistors *ACS Appl. Mater. Interfaces* **10** 22363
[31] Pizzi G, Giberntini M, Dib E, Marzani N, Iannaccone G and Fiori G 2016 Performance of arsenene and antimonene double-gate MOSFETs from first principles *Nat. Commun.* **7** 12585
[32] Campbell S A 2001 *The Science and Engineering of Microelectronic Fabrication* 2nd edn (New York: Oxford University Press)
[33] Porte L, De Villeneuve C and Phaner M 1991 Scanning tunneling microscopy observation of local damages induced on graphite surface by ion implantation *J. Vac. Sci. & Technol.* B **9** 1064–7
[34] Choi M S, Qu D, Lee D, Liu X, Watanabe K, Taniguchi T and Yoo W J 2014 Lateral MoS_2 p–n junction formed by chemical doping for use in high-performance optoelectronics *ACS Nano* **8** 9332–40
[35] He Y, Xia F, Shao Z, Zhao J and Jie J 2015 Surface charge transfer doping of monolayer phosphorene via molecular adsorption *J. Phys. Chem. Lett.* **6** 4701–10
[36] Chang H C, Lu C, Liu C L and Chen W C 2015 Single-crystal C_{60} needle/CuPc nanoparticle double floating-gate for low-voltage organic transistors based non-volatile memory devices *Adv. Mater.* **27** 27–33
[37] He Y *et al* 2019 Self-gating in semiconductor electrocatalysis *Nat. Mater.* **18** 1098–104
[38] Kandemir A, Iyikanat F and Sahin H 2019 Monitoring the crystal orientation of black-arsenic *via* vibrational spectra *J. Mater. Chem.* C **7** 1228–36
[39] Kamal C and Ezawa M 2015 Two-dimensional buckled and puckered honeycomb arsenic systems *Phys. Rev.* B **91** 085423

[40] Egerton R F 2011 *Electron Energy Loss Spectroscopy in the Electron Microscope* (Berlin: Springer) (https://doi.org/10.1007/978-1-4419-9583-4)
[41] Du Y, Liu H, Deng Y and Ye P D 2014 Device perspective for black phosphorus field-effect transistors: contact resistance, ambipolar behavior, and scaling *ACS Nano* **8** 10035–42
[42] Anugrah Y, Robbins M C, Crowell P A and Koester S J 2015 Determination of the Schottky barrier height of ferromagnetic contacts to few-layer phosphorene *Appl. Phys. Lett.* **106** 103108
[43] Das S, Zhang W, Demarteau M, Hoffmann A, Dubey M and Roelofs A 2014 Tunable transport gap in phosphorene *Nano Lett.* **14** 5733–9
[44] Das S, Chen H-Y, Penumatcha A V and Appenzeller J 2012 High performance multilayer MoS_2 transistors with scandium contacts *Nano Lett.* **13** 100–5
[45] Wu R J, Udyavara S, Ma R, Wang Y, Chhowalla M, Birol T, Koester S J, Neurock M and Mkhoyan K A 2019 Visualizing the metal-MoS_2 contacts in two-dimensional field-effect transistors with atomic resolution *Phys. Rev. Mater.* **3** 111001
[46] Park H and Kim J 2018 Enhancing ambipolar carrier transport of black phosphorus field-effect transistors with Ni–P alloy contacts *Phys. Chem. Chem. Phys.* **20** 22439–44
[47] Xia F, Wang H and Jia Y 2014 Rediscovering black phosphorus as an anisotropic layered material for optoelectronics and electronics *Nat. Commun.* **5** 4458
[48] Takagi S-H, Toriumi A, Iwase M and Tango H 1994 On the universality of inversion layer mobility in Si MOSFET's: part I-effects of substrate impurity concentration *IEEE Trans. Elect. Dev.* **41** 2357–62
[49] Grundmann M 2016 *The Physics of Semiconductors: An Introduction Including Nanophysics and Applications* (Berlin: Springer) (https://doi.org/10.1007/978-3-642-13884-3_8)
[50] Radisavljevic B and Kis A 2013 Mobility engineering and a metal–insulator transition in monolayer MoS_2 *Nat. Mater.* **12** 815–20
[51] Razavi B 1999 CMOS technology characterization for analog and RF design *IEEE J. Solid-State Circ.* **34** 268–76
[52] Wang H, Nezich D, Kong J and Palacios T 2009 Graphene frequency multipliers *IEEE Elect. Dev. Lett.* **30** 547–9
[53] Kabir H M D and Salahuddin S M 2017 A frequency multiplier using three ambipolar graphene transistors *Microelectronics J.* **70** 12–15